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THERMO-MECHANICAL STRESS ANALYSIS AND INTERFACIAL RELIABILITY FOR THROUGH-SILICON VIAS IN THREE-DIMENSIONAL INTERCONNECT STRUCTURES

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THERMO-MECHANICAL STRESS ANALYSIS AND INTERFACIAL RELIABILITY FOR THROUGH-SILICON VIAS IN THREE-DIMENSIONAL INTERCONNECT STRUCTURES

by

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Dedication

To my family

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Thermo-Mechanical Stress Analysis and Interfacial Reliability for Through-Silicon Vias in Three-Dimensional Interconnect Structures

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The University of Texas at Austin, 2011

Supervisor: Rui Huang

Continual scaling of devices and on-chip wiring has brought significant challenges for materials and processes beyond the 32-nm technology node in microelectronics. Recently, three-dimensional (3-D) integration with through-silicon vias (TSVs) has emerged as an effective solution to meet the future interconnect requirements. Among others, thermo-mechanical reliability is a key concern for the development of TSV structures used in die stacking as 3-D interconnects. In this dissertation, thermal stresses and interfacial reliability of TSV structures are analyzed by combining analytical and numerical models with experimental measurements.

First, three-dimensional near-surface stress distribution is analyzed for a simplified TSV structure consisting of a single via embedded in a silicon (Si) wafer. A semi-analytic solution is developed and compared with finite element analysis (FEA). For further study, the effects of anisotropic elasticity in Si and metal plasticity in the via on the stress distribution and deformation are investigated.

Next, by micro-Raman spectroscopy and bending beam technique, experimental measurements of the thermal stresses in TSV structures are conducted. The micro-Raman measurements characterize the local distribution of the near-surface stresses in Si around TSVs. On the other hand, the bending beam technique measures the average stress and

deformation in the TSV structures. To understand the elastic and plastic behavior of TSVs, the microstructural evolution of the Cu vias is analyzed using focused ion beam (FIB) and electron backscattering diffraction (EBSD) techniques.

To study the impacts of the thermal stresses on interfacial reliability of TSV structures, an analytical solution is developed for the steady-state energy release rate as the upper bound of the driving force for interfacial delamination. The effect of crack length and wafer thickness on the energy release rate is studied by FEA. Furthermore, to model interfacial crack nucleation, an analytical approach is developed by combining a shear lag model with a cohesive interface model.

Finally, the effects of structural designs and the variation of the constituent materials on TSV reliability are investigated. The steady state solutions for the energy release rate are developed for various TSV designs and via materials (Al, Cu, Ni, and W) to evaluate the interfacial reliability. The parameters for TSV design optimization are discussed from the perspectives of interfacial reliability.

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Chapter 1

Introduction

1.1 Background and Motivation

1.1.1 Conventional interconnects and packaging methods

In the manufacture of modern computer chips, the process flow can be divided into two steps: Front-End-Of-The-Line (FEOL) process and Back-End-Of-The-Line (BEOL) process. In the FEOL process, individual devices, such as transistors that amplify and switch electronic signals, are patterned and fabricated on the surface of a silicon wafer. Subsequently, in the BEOL process, insulating layers (dielectrics) and metal lines are deposited and fabricated to interconnect the devices on the wafer.

At the final stage of integrated circuit (IC) fabrication, the chips are integrated into chip package (or semiconductor device assembly) through several methods, such as wire bonding, die attaching, IC encapsulation, and flip chip packaging, etc.. Particularly, in the flip chip packaging method, the Si chip is flipped face down and electrically connected to the substrate through an area array of solder bumps (Fig. 1.1).

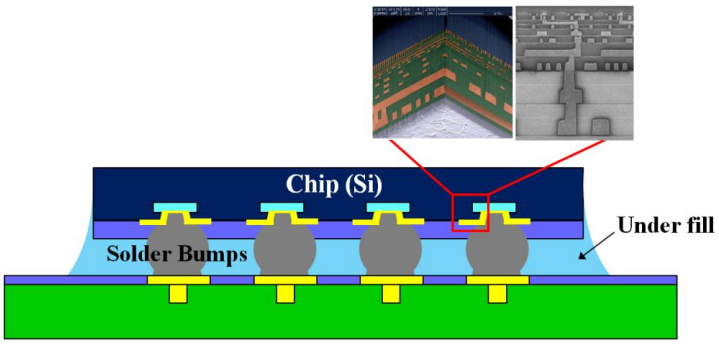


Figure 1.1: Illustration of a flip-chip packaging.

The flip chip method offers several advantages, such as smaller packaging size, large I/O density, and higher performance and reliability, and is widely used in current packaging technology.

1.1.2 Low-κ and air-gap interconnect

Over the last decade, the semiconductor industry has faced several challenges in extending Moore's law, by which the number of transistors on a single chip would double approximately in every two years [2]. The challenges are mainly due to the interconnect delay [3], also known as Resistive-capacitive (RC) delay, which can be expressed by the following formula [4]:

$$RC = 2\rho\kappa\varepsilon_o(4L^2/P^2 + L^2/T^2), \tag{1.1}$$

where $P = W + S$ is the pitch between neighboring interconnects, L is the line length, W is the interconnect line width, T is the height of the interconnect, ρ is the resistivity of the interconnect material, κ is the dielectric constant of the dielectric materials between the interconnect lines, and ε_o is the vacuum permittivity. A scaling effect on the RC delay is illustrated in Fig. 1.2.

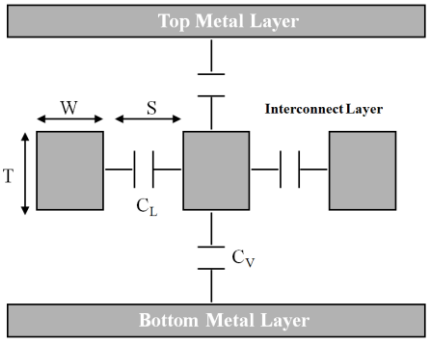
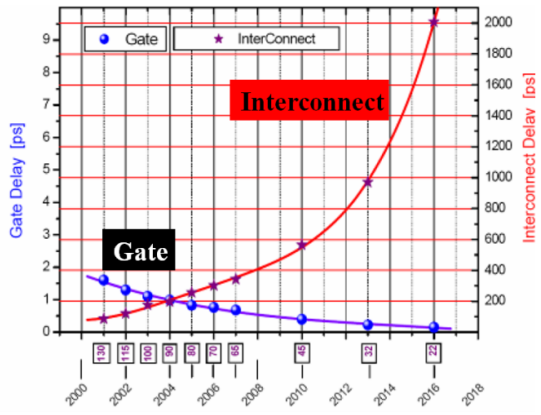
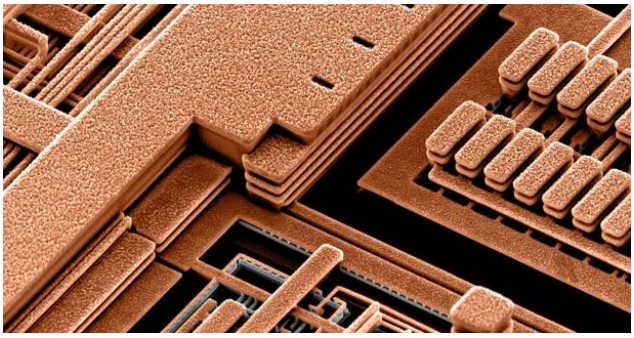


Figure 1.2: A scaling effect on RC delay in interconnects.

Figure 1.3a plots the gate and interconnect delay time as a function of the technology nodes, which clearly shows that the interconnect delay has become the dominating factor in limiting the performance of the IC chips since 2004. Since the interconnect RC delay is proportional to the resistivity of the interconnect material and the dielectric constant of the insulating layer between the interconnects, reducing ρ and/or κ will reduce the RC delay. In an effort to reduce ρ, copper has replaced aluminum as the interconnect material (Fig. 1.3b).



(a)



(b)

Figure 1.3: Delay time of interconnects (Source: IBM, 2010): (a) Comparison of delay time for gate and interconnect; (b) Cu interconnect.

To reduce the dielectric constant κ of the insulating materials, low-κ dielectric materials [5] with the dielectric constant lower than silicon dioxide ($\kappa = 3.9$) has been introduced into the interconnects. Many materials with lower dielectric constants such as fluorine-doped silicon dioxide ($\kappa = 3.5$) [6], carbon-doped silicon dioxide ($\kappa = 3.0$) [7], and porous silicon dioxide ($\kappa = 2.0$) [8], have been integrated into the IC manufacturing process. Ultimately, by formation of air-gaps ($\kappa = 1.0$) [9] in the trench dielectric levels (Fig. 1.4), the effective dielectric constant of the interconnect structure can be further reduced.

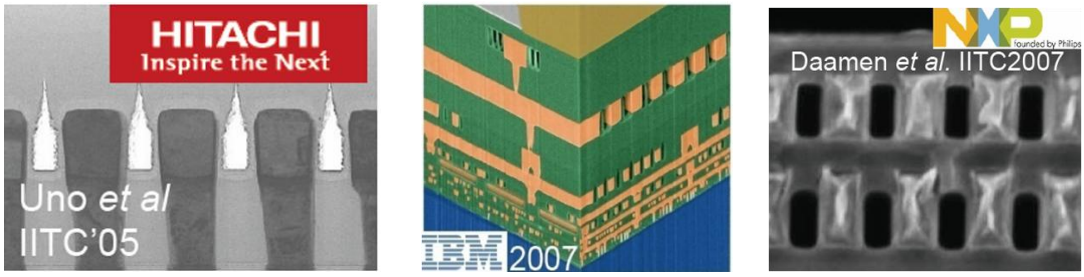


Figure 1.4: Various air-gap structures at the interconnect level.

Air gaps can be produced by non-conformal chemical vapor deposition into patterned trenches [10, 11] or by removing a sacrificial material [12, 13]. Cu interconnects using air gaps have been investigated to reduce the RC delay and crosstalk for next generation technology nodes. However, the air-gap structures at the trench level confront serious challenges concerning its structural integrity and mechanical stability [14-16]. For example, as shown in Fig. 1.5, bridging low-κ cap (or hard mask) was observed to collapse over wide air gaps during thermal decomposition of the gap forming sacrificial material [17]. Crack initiation in keyhole-shaped air gaps formed by etch-back and non-conformal refill schemes is also a potential reliability concern. As of today, the semiconductor industry still have difficulties in implementing low-κ interconnects with κ

lower than 2.5. To overcome such difficulties, a potential solution has been found in the packaging level by implementation of 3-D interconnects.

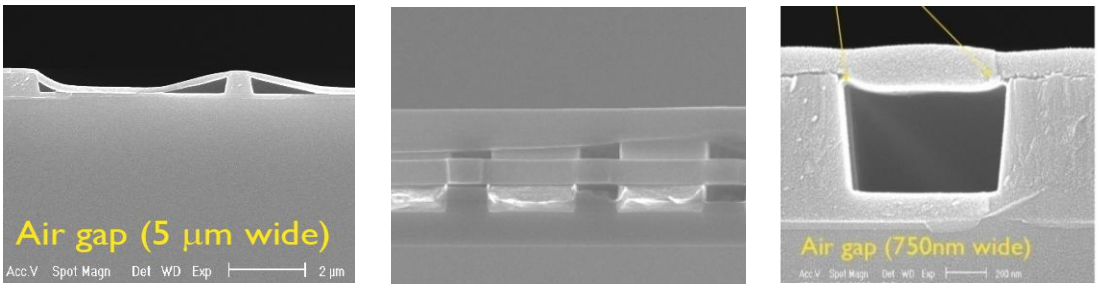
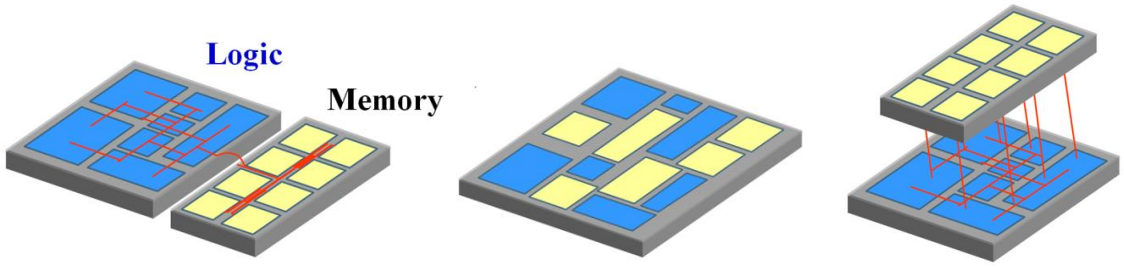


Figure 1.5: Mechanical integrity issues for air-gap interconnects [14].

1.2 3-D INTEGRATION WITH THROUGH-SILICON VIAS (TSVS)

The 3-D integration, in which two or more chips are stacked vertically, presents an effective solution to overcome the wiring limit imposed on chip performance, density and power consumption beyond the current technology [18-20]. The 3-D approach offers many advantages, such as better electrical performance and lower power consumption [21-28]. Furthermore, it allows for higher device density and smaller packaging size, which eventually would lead to reduced manufacturing cost [29]. Fig. 1.6 compares the 2-D and 3-D approaches in solving the fundamental wiring limits. Fig. 1.6a shows the 2-D SiP (System-in-Package) solution [30, 31], which has lengthy interchip connections between the logic and memory chips. Serious memory latency can exist in this case. Fig. 1.6b shows the 2-D SOC (System-on-Chip) solution [30], which improves the memory latency and device performance by combining blocks of logic and memory components in the chip. However, such approach increases the fabrication cost significantly since it requires different process technologies to the different functions. Fig. 1.6c shows the 3-D integration scheme, in which the logic and memory components are connected vertically.

In this scheme, much shorter interconnects are needed, and therefore the memory latency can be significantly reduced and the chip performance improved. A critical structural element in the 3-D integration is the through-silicon via (TSV) [32-36] as shown in Fig. 1.7, which replaces the edge wiring in the 2-D schemes by vertical connections between the stacked dies. The use of TSVs in 3-D integration can effectively improve system performance and reduce manufacturing costs.

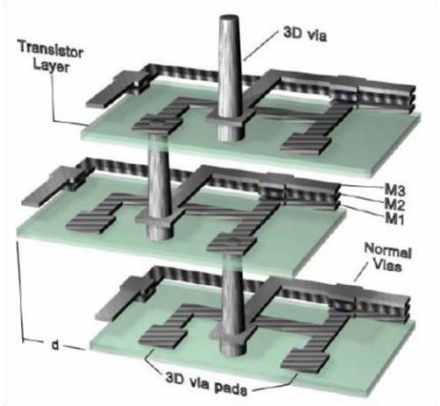


(a) (b) (c)

Figure 1.6: Schematic diagrams showing the difference between 2-D and 3-D interconnects: (a) 2-D SiP integration; (b) SOC integration; (c) 3-D integration. (Source: Beyne [37]).

1.2.1 Process flow for TSV fabrication

The fabrication of TSVs involves three key processes [38-41]: 1) via hole etching, 2) TSV filling by electroplating, and 3) Si wafer thinning and wafer bonding/debonding. For a reliable and efficient TSV fabrication, each of the three processes needs to be optimized. For example, the TSV structure demands high depth-to-diameter aspect ratio (AR~10) via holes. In general, DRIE (Deep reactive-ion etching) process, also known as the “Bosch” process, is applied for via etching.



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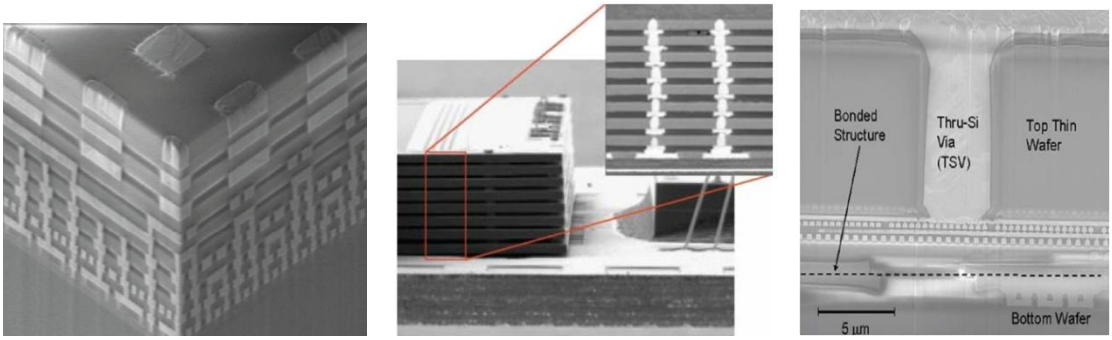
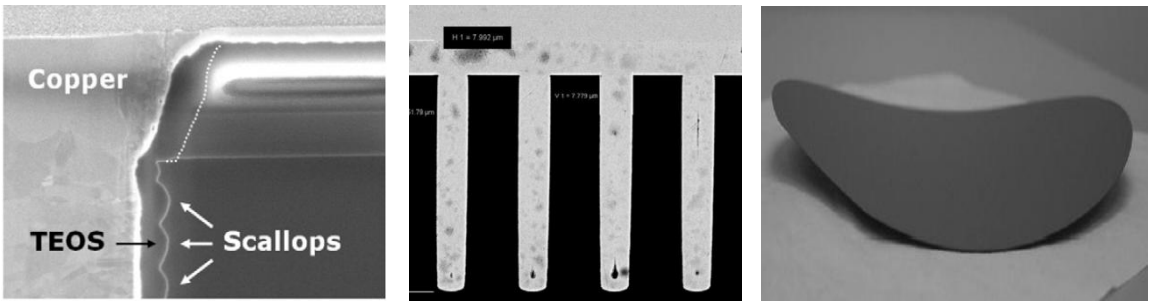


(b)

Figure 1.7: 3-D integration using TSV structures; (a) Illustration of Through-Silicon-Vias (TSV); (b) TSV samples (Source: NIST/Samsung/Intel).

However, careful control of the Bosch process is needed to prevent formation of scallop-shaped sidewalls (Fig. 1.8a) [38, 42], as the scalloped contours not only prevent a conformal barrier and seed layer deposition, but also increase the Cu diffusion into silicon despite the presence of the barrier layer [43]. During the electroplating of Cu, voids can sometimes form inside the TSVs (Fig. 1.8b) [44], directly affecting the device reliability. In addition, the thinning-down process of the Si substrate by chemical-mechanical polishing (CMP) could cause wafer warpage (Fig. 1.8c) [45], which leads to subsequent problems in 3-D stacking. To address various processing issues, several

processing flows have been investigated [38, 46-48]. As of today, two TSV integration processes are mostly used in the semiconductor industry; 'via-middle' and 'via-last' processes. The main difference in these two processes is the sequence of the TSV formation relative to the wafer thinning and wafer bonding/debonding processes.



(a) (b) (c)

Figure 1.8: Processing issues: Scallops at sidewall [38]; Voids inside TSV [44]; Wafer warpage [49].

Via-middle process

Fig. 1.9 schematically illustrates the via-middle process, which is performed following the FEOL fabrication process. A typical via-middle process flow to fabricate TSVs with a diameter of 10 μm and a depth of 50 μm in the Si substrate is described as the following. First, lithography is conducted to pattern the via openings across the wafer. Next, DRIE is used to create the via holes of desired dimensions. This is then followed by deposition of an oxide liner of around 1 μm thick. The oxide layer (dielectric layer) reduces capacitance and improves electrical isolation between the TSVs and the Si substrate. In some cases, instead of oxide, polymeric dielectric materials [50, 51] such as benzocyclobutene (BCB) or parylene have been deposited as the sidewall insulators. To prevent diffusion of Cu into the Si substrate, a thin barrier layer (~50nm) of Ta/TaN or

Ti/TiN is deposited. For Cu electroplating, a thin Cu seed layer is first deposited in the via and then the vias are filled by electroplating process. A subsequent annealing step could be applied to stabilize the Cu grain structures and relax the residual stresses for further processing that follows. At the final stage of the TSV fabrication, CMP is conducted to remove the Cu overburden, Ta/TaN layers, and oxide liner, and to planarize the wafer surface. The fabrication of TSV structures is followed by the BEOL process in which interconnects are made and bonding pads are patterned. Finally, the Si substrate is thinned down up to the optimized TSV height (~50 μm).

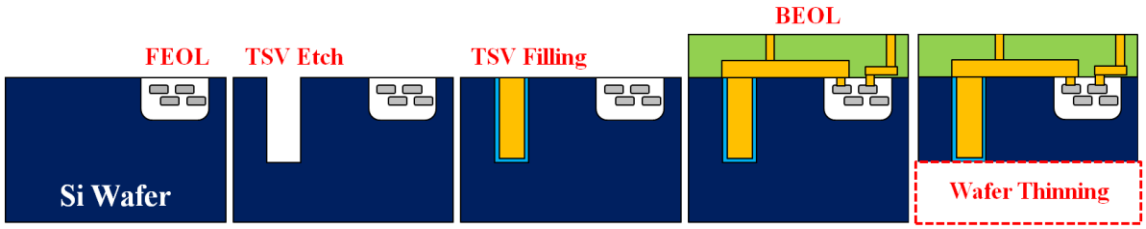


Figure 1.9: Via-middle process for TSV structures.

Via-last process

The via-last process also involves similar processes as described before, including drilling of via holes and deposition of dielectric layer and barrier layers. However, although the final structure constructed by the via-middle or via-last process could be the same, the sequence of processes in the via-last process (Fig. 1.10) is quite different from the via-middle process. In the via-last process, both FEOL and BEOL structures are first fabricated on the Si wafer. Then, the wafer is thinned down up to the depth that is targeted for the TSV height. This is then followed by etching of the via holes from the back side of wafer to reach the interface of BEOL interconnect lines, and filling the holes by the sequence of dielectric layer, Ta/TaN barrier layer, Cu seed, electroplating of Cu, and finally a CMP process.

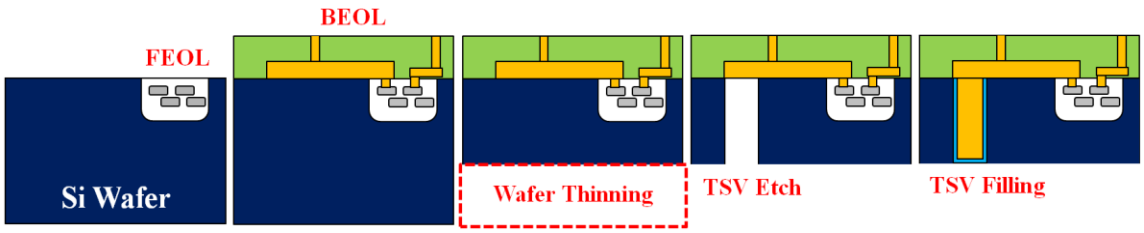


Figure 1.10: Via-last process for TSV structures.

1.2.2 Mechanical issues in TSV structures

While the 3-D integration with TSVs offers a promising solution for future technology nodes, serious mechanical reliability concerns have been raised. Due to the CTE mismatch between the via materials and Si, thermal stresses are ubiquitously induced during processing and thermal cycling of the TSV structures [52]. The thermal stresses can cause interfacial delamination, cracking of Si, and degradation of stress-sensitive devices. Therefore, it is essential to understand the characteristics of thermo-mechanical stresses developed in the TSV structures and the impacts on reliability for successful implementation of 3-D integration.

Extrusion of Cu vias is frequently observed in the TSV structures undergoing high temperature excursion. The via pop-up phenomenon can cause interfacial failure of a TSV (Figure 1.11a) or/and cracking in Si near the lower ends of TSVs (Fig. 1.11b) during the thermal processing [53]. The via extrusion can be accompanied by interfacial delamination, as shown in Fig. 1.11c. Moreover, the effects of Cu plasticity have drawn considerable attention since it may also play an important role in via extrusion.

To understand the failure mechanisms in the TSV structures, it is essential to experimentally characterize the induced stresses and material behaviors under the thermomechanical conditions for TSV fabrication. Several experimental approaches have been applied for this purpose. For example, indentation tests have been performed to

measure the residual stress of TSV structures [54, 55]. As a nondestructive method, Raman spectroscopy has been applied to measure the stress in Si surrounding the TSVs [56-61]. Both the indentation and Raman measurements can be used to determine the characteristics of process-induced stresses around TSVs near the wafer surface. More recently, the bending beam curvature technique has been introduced to measure the average stress in the TSV structures [62], which showed clearly elastic and inelastic behavior during thermal cycling. Stress measurements by the bending beam technique and Raman spectroscopy will be the focus of Chapter 3 in this dissertation.

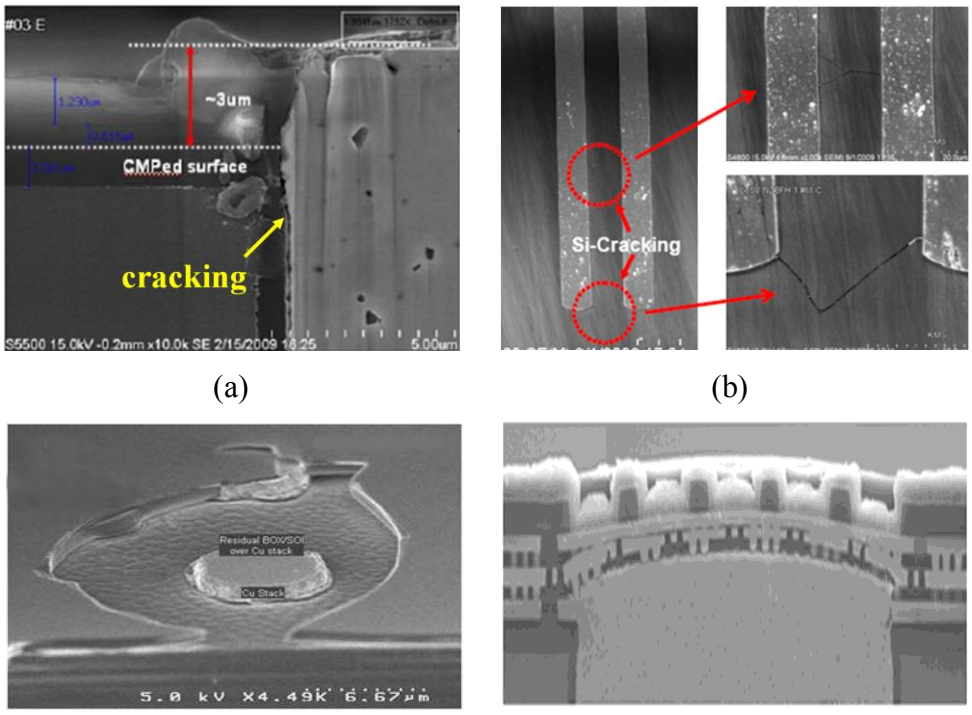


Figure 1.11: Mechanical issues in TSV structures (Source: Samsung [53]): (a) Interfacial delamination; (b) Silicon cracking; (c) Via extrusion (Pop-up).

1.3 SCOPE OF DISSERTATION

In this dissertation, analytic and numerical approaches are applied, along with experimental measurements, to study the thermo-mechanical issues in TSV structures for 3-D integration. Thermal stresses and interfacial reliability of TSV structures are analyzed. Experimental measurements of the stresses in the TSV structures are conducted by micro-Raman spectroscopy and bending beam technique. Together, a comprehensive understanding is established for the thermomechanical stress and reliability of TSV structures, based on which reliable design and processing are suggested. This dissertation is organized as follows.

As an introduction, Chapter 1 presents a brief review of the background and motivation for this work. The conventional interconnect and packaging schemes are briefly reviewed, and the current challenging issues related to the interconnects are discussed. In the course of the technology trend to overcome the challenges, the advantages of 3D integration are introduced and the fabrication processes are described.

Chapter 2 presents a semi-analytic solution for the stress analysis near the wafer surface, assuming an isolated TSV embedded in the silicon wafer. Then finite-element analysis is performed to compare with the semi-analytical solution. The effects of anisotropic elasticity in Si and Cu plasticity on the stress distribution are analyzed.

In Chapter 3, two experimental methods, micro-Raman spectroscopy and bending beam curvature technique, are used to measure thermal stresses in the TSV structures. The micro-Raman spectroscopy measures a certain combination of the near-surface stresses in Si. On the other hand, the bending beam technique measures the average stress in the specimen containing a periodic array of Cu TSVs. Moreover, microstructural evolution of the Cu TSVs after thermal cycles are studied using focused ion beam (FIB) and electron backscattering diffraction (EBSD).

Chapter 4 focuses on the interfacial reliability of TSV. An analytical solution is developed for the steady-state energy release rate as the upper bound for the fracture driving force. The effect of crack length on the energy release rate is studied by finite element calculations. Furthermore, to model interfacial crack nucleation, an analytical approach is developed by combining a shear lag model with a cohesive interface model.

In Chapter 5, the effects of structural designs (fully-filled TSV, annular TSV, TSV with a dielectric layer, and TSV with nail head) and the variation of the constituent materials (Cu, Al, Ni, W) on TSV reliability are investigated. Based on these results, suggestions are made for reliable design and processing of TSV structures.

In conclusion, Chapter 6 summarizes the results from the present study and suggests potential directions for future works.

Chapter 2

Three-Dimensional Stress Analysis for TSV Structures

Use of TSVs in 3-D integration can effectively improve system performance and reduce manufacturing costs [29]. The TSVs may assume various structural configurations such as fully filled TSVs, annular TSVs, TSVs with 'nail head', and TSVs with dielectric buffer layers (see Fig. 1). Due to the mismatch in the coefficients of thermal expansion (CTEs) of the via materials and Si, thermal stresses are ubiquitously induced during processing and thermal cycling of TSV structures, which can potentially degrade the performance of stress-sensitive devices around the TSVs [63] or drive crack growth in 3-D interconnects [42, 64-67]. Therefore, the success of 3-D integration largely relies on the characteristics of thermo-mechanical stresses developed in the system and its impact on reliability. Finite element methods have been used to numerically analyze the thermo-mechanical stresses in 3-D integrated structures [42, 64-67], typically complicated by specific material processes and structural designs. In addition to these numerical studies, a simple analytical approach based on a two-dimensional (2-D) model was employed to analyze the thermo-mechanical interactions in TSV arrays [68]. However, the 2-D solution does not capture the 3-D nature of the stress field near the wafer surface around a TSV. Determination of the 3-D near-surface stress distribution is critical due to the fact that the active devices are usually located near the wafer surface. In this Chapter, a semi-analytic 3-D solution is developed for an isolated TSV embedded in the silicon wafer (Fig. 2.1a), which compares closely with numerical results obtained by finite element analysis (FEA) for TSV structures with relatively thick wafers. Then, effect of wafer thickness on stress distributions is investigated by finite element analysis. Furthermore,

effects of anisotropic elasticity of Si and plasticity of the via material are discussed based on numerical results.

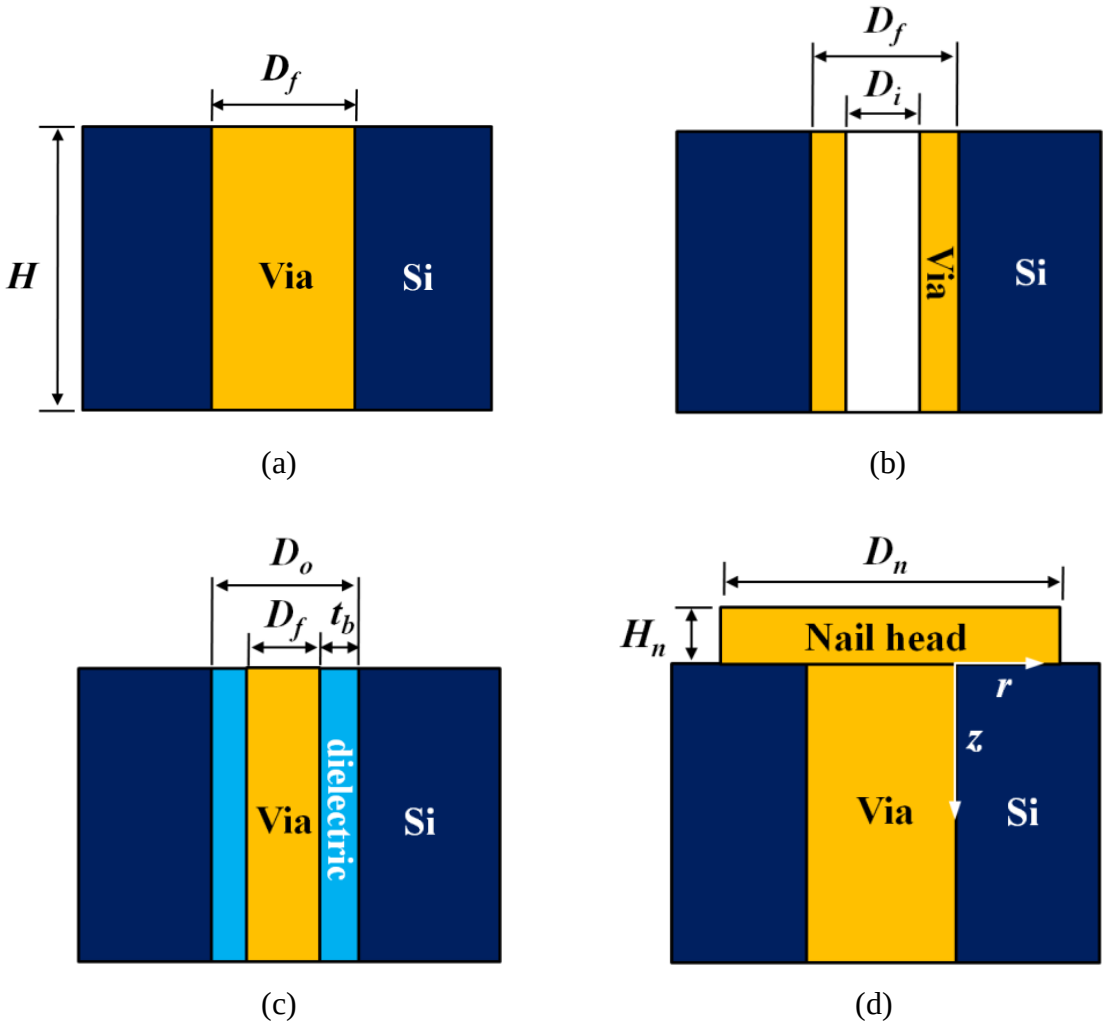


Figure 2.1: Schematics of through-silicon vias (TSVs) in various structural forms: (a) Fully filled TSV; (b) Annular TSV; (c) TSV with a dielectric buffer; (d) TSV with a nail head.

2.1 A SEMI-ANALYTICAL SOLUTION

Consider a single cylindrical TSV embedded in an infinite Si wafer (Fig. 2.1a). As a prerequisite for the study of stress-related phenomena, it is assumed in this section that

all materials are isotropic and linearly elastic. Under the assumption of linear elasticity, the stress field in the TSV structure induced by differential thermal expansion can be obtained by superposition of the two problems sketched in Fig. 2.2. In Problem A (Fig. 2.2b), the system is subjected to a thermal loading (ΔT) and a uniform stress (σ_z) on the surfaces of the via, so that the stress field is homogeneous in the via. To recover the traction-free boundary condition on the surfaces in the original problem, the normal stress on the surface is removed by superimposing Problem B (Fig. 2.2c), in which a pressure of the same magnitude ($p = \sigma_z$) is applied at both ends of the via, but no thermal load.

Problem A can be solved analytically, while an approximate solution to Problem B can be obtained semi-analytically. The same approach was taken previously to determine the stress field in fiber-reinforced intermetallic composites [69]. The solution to Problem A in Fig. 2.2b is identical to the 2-D plane-strain solution to the classical Lame problem in elasticity [70]. The stress in the via is uniform and tri-axial, with the following components:

$$\sigma_r^A = \sigma_\theta^A = \frac{-E_f \varepsilon_T}{1-2\nu_f + \dfrac{1+\nu_m}{1+\nu_f}\dfrac{E_f}{E_m}}, \tag{2.1}$$

$$\sigma_z^A = -E_f \varepsilon_T \left[\frac{1+\dfrac{1+\nu_m}{1+\nu_f}\dfrac{E_f}{E_m}}{1-2\nu_f + \dfrac{1+\nu_m}{1+\nu_f}\dfrac{E_f}{E_m}} \right], \tag{2.2}$$

where σ_r, σ_θ, and σ_z are the radial, circumferential, and axial stresses, respectively, and $\varepsilon_T = (\alpha_f - \alpha_m)\Delta T$ is the mismatch strain due to the thermal load ΔT. The material properties, α, E, ν, are the coefficient of thermal expansion (CTE), Young's modulus, and Poisson's ratio, with the subscripts *f* and *m* for the via (fiber) and Si

(matrix), respectively. The corresponding stress field in Si ($r > D_f/2$) is non-uniform and bi-axial:

$$\sigma_r^A = -\sigma_\theta^A = \frac{-E_f \varepsilon_T}{1-2\nu_f + \frac{1+\nu_m}{1+\nu_f}\frac{E_f}{E_m}} \left(\frac{D_f}{2r}\right)^2, \tag{2.3}$$

where D_f is the diameter of the TSV and r is the radial coordinate measured from the center of the via. The stress field in Eqs. (2.1-3) can be simplified by neglecting the elastic mismatch between the via and Si, with $E_f = E_m = E$ and $\nu_f = \nu_m = \nu$ as given in the previous studies [68, 71]. The above 2-D solution do not satisfy the traction-free boundary condition on the surfaces in the original problem (Fig. 2.2a) because of presence of the axial stress (σ_z^A) in the via. This is corrected by superimposing Problem B in Fig. 2.2c, with a uniform axial stress of the same magnitude acting at both ends of the TSV in the opposite direction (i.e., $p = \sigma_z^A$).

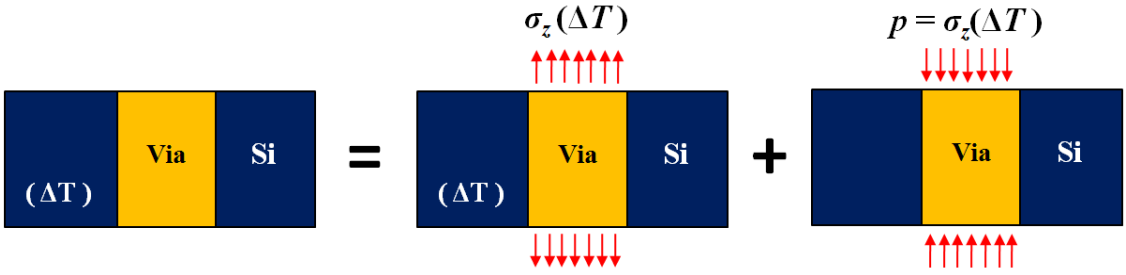


Figure 2.2: Illustration of the method of superposition to obtain a semi-analytical solution for thermal stresses in a TSV structure: (a) the original problem, with a thermal load and traction-free surfaces; (b) Problem A, with a thermal load and surface traction; (c) Problem B, with surface load only.

The stress field due to the surface pressure is typically localized near the ends of the via. Thus, the stress distribution from the 2-D solution in Eqs. (2.1-3) is an accurate solution at locations far away from the ends of the TSV, especially for high aspect-ratio

(height/diameter or H/D_f) TSVs embedded in a thick wafer. However, the correction due to Problem B renders a significantly different stress distribution near the wafer surface around the TSV. For a relatively thin wafer, the stress in the entire via and its surrounding can be affected and thus different from the 2-D solution. In the following, a semi-analytical solution to Problem B for a thick wafer is first developed, and then the effect of wafer thickness is studied by finite element analysis (FEA).

Focusing on the near-surface stress field for Problem B in Fig. 2.2c, consider a semi-infinite wafer subjected to a uniform pressure on the surface over a circular area of diameter D_f. For simplicity, neglect the elastic mismatch between the via and Si, so that $p=\sigma_z^A=-E\varepsilon_T/(1-\nu)$. Consequently, the solution can be obtained in an integral form based on the 3-D solution to the classical Boussinesq problem [70, 72]. The following stress components are obtained with an auxiliary coordinate shown in Fig. 2.3:

$$\sigma_z^B(r,z)=\frac{E\varepsilon_T}{1-\nu}\int_0^{2\pi}\int_0^{\frac{D_f}{2}}\frac{3z^3\rho d\rho d\theta}{2\pi R^5}, \tag{2.4}$$

$$\sigma_{rz}^B(r,z)=\frac{E\varepsilon_T}{1-\nu}\int_0^{2\pi}\int_0^{\frac{D_f}{2}}\frac{3z^2(r-\rho\cos\theta)\rho d\rho d\theta}{2\pi R^5}, \tag{2.5}$$

$$\begin{aligned}\sigma_r^B(r,z)=\frac{-E\varepsilon_T}{2\pi(1-\nu)}\int_0^{\frac{D_f}{2}}\int_0^{2\pi}\Bigg[&\left(\frac{1-2\nu}{R^2+Rz}-\frac{3z(R^2-z^2)}{R^5}\right)\cos^2\beta\\&+\left(\frac{z}{R^3}-\frac{1}{R^2+Rz}\right)(1-2\nu)\sin^2\beta\Bigg]\rho d\rho d\theta\end{aligned}, \tag{2.6}$$

$$\begin{aligned}\sigma_\theta^B(r,z)=\frac{-E\varepsilon_T}{2\pi(1-\nu)}\int_0^{\frac{D_f}{2}}\int_0^{2\pi}\Bigg[&\left(\frac{1-2\nu}{R^2+zR}-\frac{3z(R^2-z^2)}{R^5}\right)\sin^2\beta\\&+\left(\frac{z}{R^3}-\frac{1}{R^2+zR}\right)(1-2\nu)\cos^2\beta\Bigg]\rho d\rho d\theta\end{aligned}, \tag{2.7}$$

where $R=\sqrt{z^2+\rho^2+r^2-2\rho r\cos\theta}$ and $\beta=\tan^{-1}\left(\frac{\rho\sin\theta}{r-\rho\cos\theta}\right)$. The stress field for Problem B is axi-symmetric, varying with both r and z in the cylindrical coordinate.

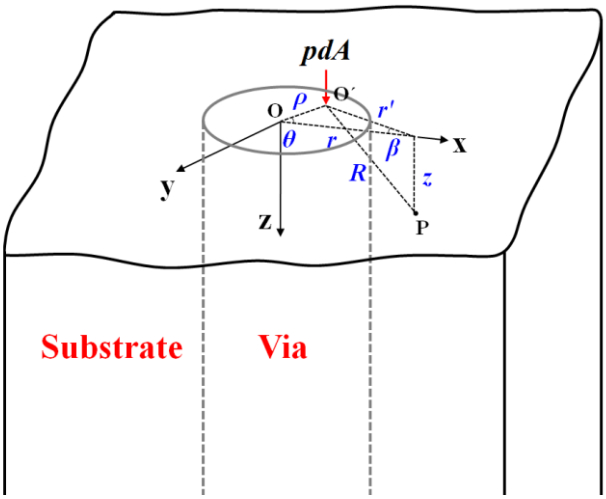


Figure 2.3: An elastic half space subject to surface pressure over a circular area.

Finally, the near-surface stress distribution around the via is obtained by adding the stress distributions in Eqs. (2.4-7) onto Eqs. (2.1-3) for both the via and the Si wafer, i.e., $\sigma_z = \sigma_z^A + \sigma_z^B$, etc. The contours of the overall stress distribution are plotted in Figure 2.4, where the stress magnitude is normalized by the pressure $p = -E\varepsilon_T / (1-\nu)$ and the integrals in Eqs. (2.4-7) are evaluated numerically by the method of quadratic interpolation [73].

Figure 2.4a shows that the normal stress σ_z is zero on the surface ($z = 0$), as required by the traction-free boundary condition. The normal stress is non-uniform in the via and Si near the surface. Unlike the 2-D solution, the shear stress (σ_{zr}) is not zero near the end of the via (Fig. 2.4b). In fact, a concentration of the shear stress is predicted at the junction between the surface ($z = 0$) and via/Si interface ($r = D_f / 2$), which can contribute to the driving force for interfacial delamination. The distributions of the radial stress (σ_r) and the circumferential stress (σ_θ) near the end of the TSV (Figs. 2.4c and 4d) are also distinct from the predictions by the 2-D solution. Depending on the sign of

the thermal mismatch strain, $\varepsilon_T = (\alpha_f - \alpha_m)\Delta T$, the stresses can be either tensile or compressive. For example, if $\alpha_f > \alpha_m$, $p < 0$ for heating ($\Delta T > 0$) and $p > 0$ for cooling ($\Delta T < 0$). For the case of cooling, the radial stress is tensile along the via/Si interface, which can contribute to the driving force for interfacial delamination. The radial stress is also tensile in Si near the surface, which may cause circumferential cracking (C-cracks) of the Si. During heating, the circumferential stress is tensile in Si, which may cause radial cracks (R-cracks) in Si. For both heating and cooling, the presence of the shear stress (σ_{rz}) along the TSV/Si interface can cause interfacial failure by delamination.

At the center of the via ($r = 0$), the stresses can be obtained in closed form as follows [70]:

$$\sigma_z(z; r=0) = -\frac{E\varepsilon_T}{1-\nu}\frac{z^3}{\left(z^2 + D_f^2/4\right)^{3/2}}, \tag{2.8}$$

$$\begin{aligned}\sigma_r(z; r=0) &= \sigma_\theta(z; r=0) \\ &= -\frac{E\varepsilon_T}{2(1-\nu)}\left[-2\nu + \frac{2(1+\nu)z}{\sqrt{z^2 + D_f^2/4}} - \frac{z^3}{\left(z^2 + D_f^2/4\right)^{3/2}}\right].\end{aligned} \tag{2.9}$$

The variation of the stresses in the via could be important for the study of plastic yielding and stress migration in TSVs.

On the Si surface ($z = 0$ and $r > D_f/2$), it is found that $\sigma_r + \sigma_\theta = 0$, which suggests weak Raman shifts for stress measurements using micro-Raman spectroscopy [74] as will be discussed further in Chapter 3. It is also important to recognize the variation of the near-surface stresses in the *z*-direction, since the Raman measurement typically averages over certain depth below the surface. Depending on the magnitudes and signs of the stresses, channeling cracks may grow at the Si surface near the TSV, in

either the radial or the circumferential direction. The near-surface stresses can also degrade the electrical performance of the devices located near the Si surface and the TSV [64]. Thus, understanding the characteristics of the near-surface stresses in Si is essential for the design of the keep-out zone [64, 67] around the TSV to mitigate the impact of stresses on the device performance.

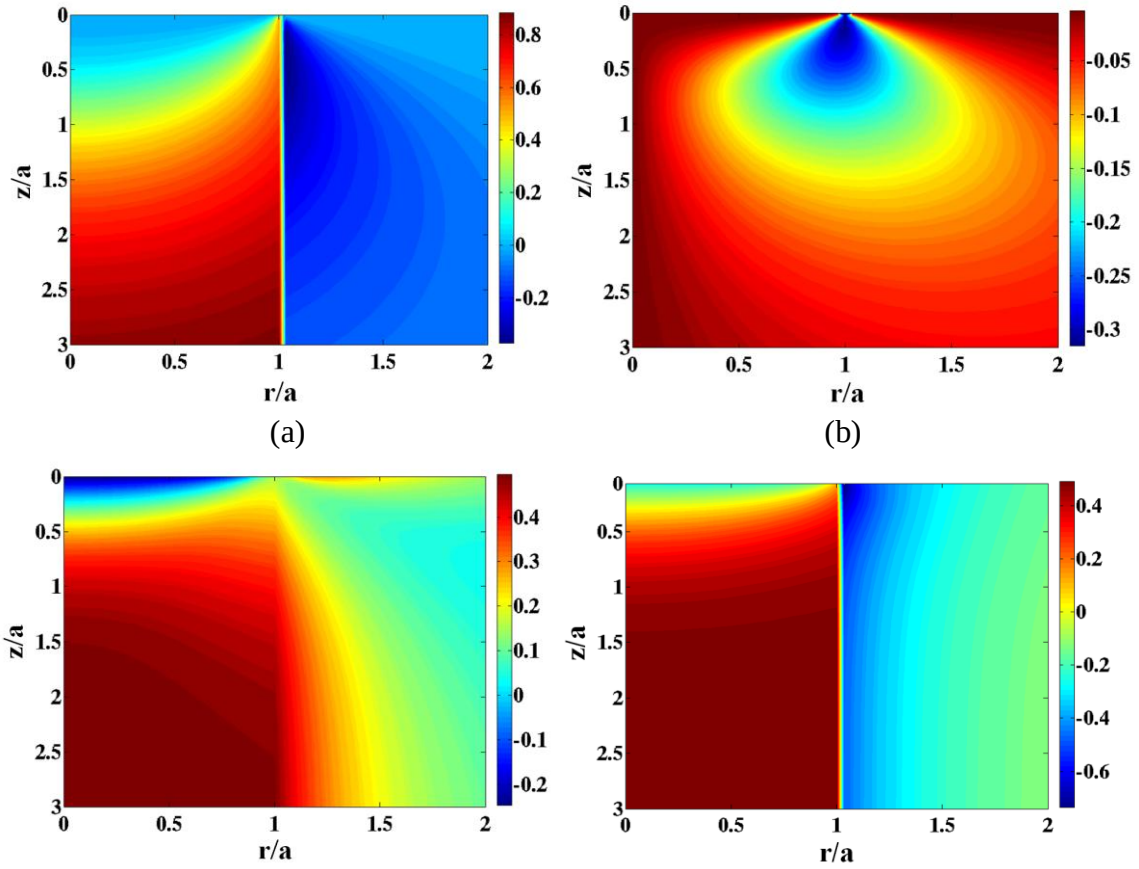


Figure 2.4: Near-surface stress distributions predicted by the semi-analytical solution. The stress magnitudes are normalized by $p = -E\varepsilon_T / (1-\nu)$, and the radial and depth coordinates (r and z) are normalized by the via radius $a = D_f / 2$: (a) out-of plane stress (σ_z); (b) shear stress (σ_{rz}); (c) radial stress (σ_r); (d) circumferential stress (σ_θ).

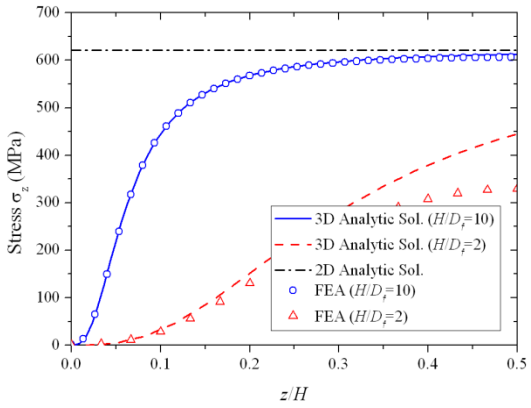
2.2 FINITE ELEMENT ANALYSIS (FEA)

To verify the semi-analytic solution developed in the previous section, finite element analysis (FEA) is performed using the commercial package, ABAQUS (v6.8). Since the thickness of the Si wafer is one of the key design parameters for the TSV structure, the effect of wafer thickness on thermal stress distribution is examined by FEA models with two different thicknesses. The model structure is shown in Fig. 2.1a, with the TSV diameter $D_f = 30\,\mu\text{m}$ and the wafer thickness H=300 μm and 60 μm. In the FEA models, linear 3-D solid elements (C3D8R) with the size of 0.5 μm ×1 μm are used. A negative thermal loading (cooling), $\Delta T = -250$ ℃, is assumed. The material properties are: $E_f = E_m = 110\,\text{GPa}$, $\nu_f = \nu_m = 0.35$, and $\alpha_f = 17$ ppm/℃ and $\alpha_m = 2.3$ ppm/℃. The model is an approximation to a Cu TSV in Si, neglecting the elastic mismatch between Cu and Si. In practice a thin barrier layer is typically deposited between the Cu via and Si, which has negligible effects on the stress distribution and is thus ignored here.

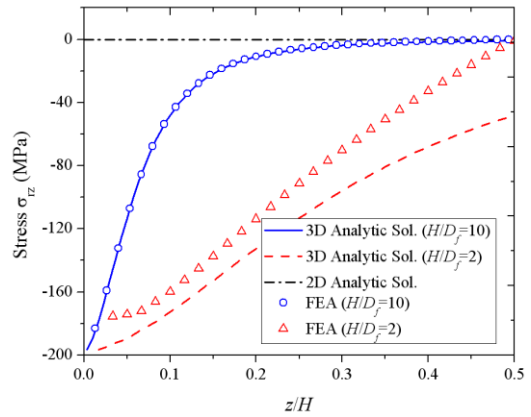
Figure 2.5 shows the FEA results, in comparison with the semi-analytical solution. First, the axial stress (σ_z) along the center line of the TSV (r = 0) shows the transition from zero stress at the surface (z = 0) to a tensile stress away from the surface (Fig. 2.5a). For the thick wafer ($H / D_f = 10$), the FEA result shows excellent agreement with the analytical solution in Eq. (2.8), both approaching the 2-D solution (the dashed line) away from the surface. For the thin wafer ($H / D_f = 2$), however, the axial stress in the TSV is significantly lower, due to close proximity of the two free surfaces. The shear and radial stresses along the TSV/Si interface ($r = D_f / 2$) are shown in Figs. 2.5b and 2.5c, respectively. Again, the semi-analytical solution compares closely with the FEA results for the thick wafer. By symmetry, the shear stress is zero at the mid-plane of the wafer ($z / H = 0.5$). Based on an asymptotic analysis of the semi-analytical solution [75], the magnitude of the shear stress at the interface approaches a finite value ($\sigma_{rz} \to -p / \pi$)

at the surface ($z = 0$). In between, the variation of the shear stress depends on the wafer thickness. Similarly, the radial stress (σ_r) at the interface asymptotically approaches a finite value ($\sigma_r \to (0.5 - v)p$) at z=0 and approaches the 2-D solution (the dashed line, $\sigma_r \to 0.5p$) far away from the surface. For the thinner wafer, the radial stress is slightly higher near the surface but is lower elsewhere. In the case of cooling ($\Delta T < 0$), both the shear stress and the tensile radial stress contribute to the driving force for interfacial delamination, as discussed in Chapter 4. It is seen from Fig. 2.5 that the 2-D plane-strain solution only predicts stresses far away from the wafer surface, while the semi-analytical 3-D solution is a good approximation everywhere for relatively thick wafers (e.g., $H / D_f > 10$). Neither solution is applicable for very thin wafers ($H / D_f < 2$).

In addition to the wafer thickness effect, FEA models have also been used to study the following effects on stresses in TSV structures: (1) different material properties for the via and Si, including anisotropic elasticity of Si and plasticity of the via material; (2) different TSV structures; and (3) periodic TSV arrays. The remainder of this chapter focuses on the effects of anisotropic elasticity in Si and plasticity in the via material, and the other results are discussed in the subsequent Chapters.



(a)



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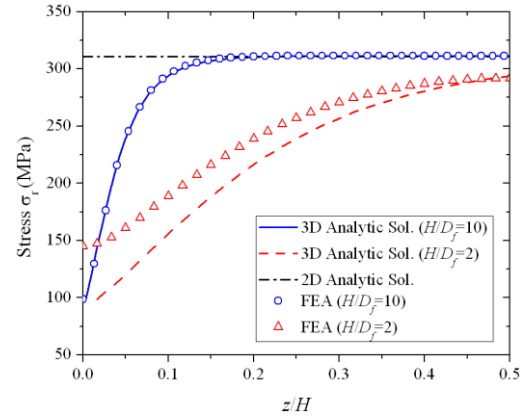


(c)

Figure 2.5: Effect of wafer thickness on stress distributions ($D_f = 30\,\mu\text{m}$ and $\Delta T = -250$ ºC): (a) Axial stress at the via center ($r = 0$); (b) Shear stress at the TSV/Si interface ($r = D_f / 2$); (c) Radial stress at the TSV/Si interface ($r = D_f / 2$).

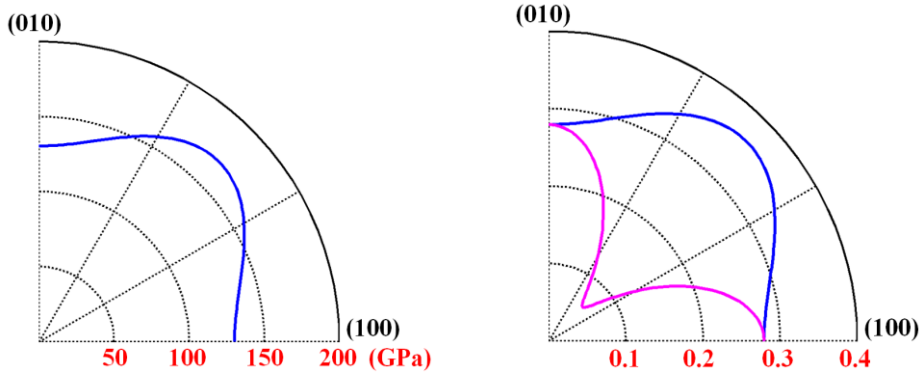
2.3 EFFECT OF ELASTIC ANISOTROPY OF SI

The orientation of Si wafer is very important for the electronic devices since the mechanical and electronic properties of Si are anisotropic. In this section, the effect of anisotropic elastic properties of silicon on thermal stresses is evaluated. Specifically, the (001) Si wafer, which is the most common type of wafers, is considered in comparison with the isotropic model.

The stiffness matrix of the (001) Si wafer is [76]

$$C_{(001)} = \begin{bmatrix} 166.2 & 64.4 & 64.4 & 0 & 0 & 0 \\ 64.4 & 166.2 & 64.4 & 0 & 0 & 0 \\ 64.4 & 64.4 & 166.2 & 0 & 0 & 0 \\ 0 & 0 & 0 & 79.8 & 0 & 0 \\ 0 & 0 & 0 & 0 & 79.8 & 0 \\ 0 & 0 & 0 & 0 & 0 & 79.8 \end{bmatrix} \text{GPa} \qquad (2.10)$$

The anisotropic elastic property of Si is illustrated by the polar plots of the elastic modulus and Poisson's ratio in Fig. 2.6. In comparison, the polar plots for an isotropic material would be circular with identical elastic moduli in all directions.

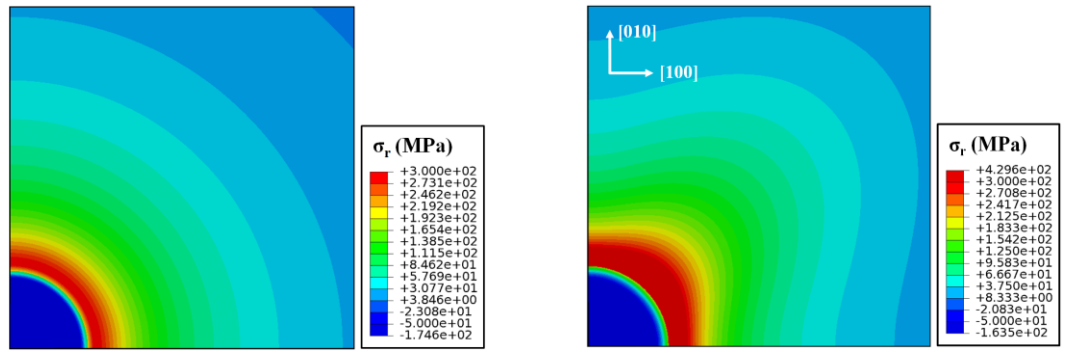


(a) (b)

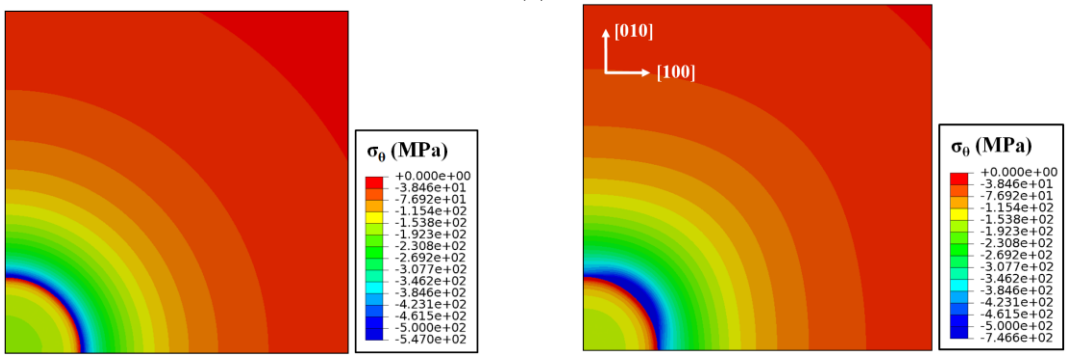
Figure 2.6: Elastic properties for (001) Si: (a) Young's modulus; (b) Poisson's ratio (the pink line for the in-plane Poisson's ratio, and blue line for the out-of plane Poisson's ratio).

In the FEA analysis, Si is modeled as an anisotropic elastic material with the stiffness matrix in Eq. (2.10) and Cu is modeled as an isotropic elastic material with $E = 110\,\text{GPa}$ and $\nu = 0.35$. The result is compared to an isotropic model in which the elastic moduli of Si are taken to be $E = 130\,\text{GPa}$ and $\nu = 0.28$. The FEA model uses the same geometry and boundary conditions as described in the previous section for an isolated TSV with $\Delta T = -250\,^{\circ}\text{C}$. In Fig. 2.7a-b, the radial and circumferential stresses on the wafer surface ($z = 0$) are plotted as contours for the isotropic and anisotropic models. The result from the isotropic model is axi-symmetric, with concentric circular contours for both the radial and circumferential stresses. By symmetry, the in-plane shear stress ($\sigma_{r\theta}$) in Fig. 7c is zero everywhere in the isotropic model. However, when the anisotropic elastic property of Si is considered, the stress distribution in the (001) Si is no longer axi-symmetric. Instead, it exhibits a four-fold symmetry, reflecting the cubic symmetry of the Si crystal. In addition, the in-plane shear stresses at certain regions are not zero any more.

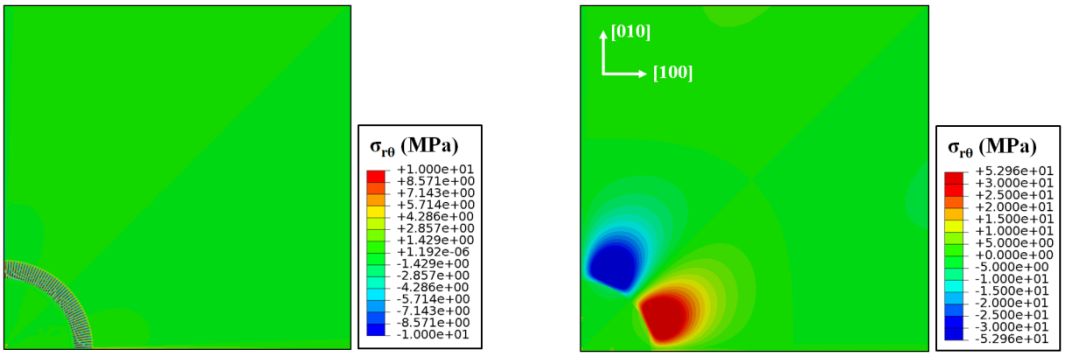
These results suggest that, due to the elastic anisotropy of Si, the near-surface stress distribution to be measured by Raman spectroscopy is directional-dependent. In Chapter 3, the anisotropic effect on the Raman measurement will be further discussed.



(a)



(b)



(c)

Figure 2.7: Effect of anisotropic elasticity on stress distributions ($D_f = 30\,\mu\text{m}$ and $\Delta T = -250\,^{\circ}\text{C}$): (a) Radial stress, σ_r for isotropic Si (left) and (001) Si (right); (b) Circumferential stress, σ_θ for isotropic Si (left) and (001) Si (right); (c) Shear stress, $\sigma_{r\theta}$ for isotropic Si (left) and (001) Si (right).

2.4 EFFECT OF PLASTICITY

The fabrication of TSV structures typically requires processing at high temperatures. Depending on the fabrication process, materials in the via could experience plasticity by a positive or a negative thermal load. For example, after Cu plating, the TSV structures need to be heat up to temperatures as high as 400^{o}C for the deposition of additional passivation layers (TEOS or SiN). During such processes, the TSVs undergo positive thermal loads that are large enough to cause plasticity in the via. Plasticity could also develop in the via during cooling process if stress relaxation occurs at the high temperatures. As a result, the plasticity effects could significantly change the stress behavior and thus impact the thermomechanical reliability for TSV structures. In this section, the effects of plasticity on TSV structures are investigated for both positive and negative thermal loads.

A finite element model is used to study the effect of plasticity in the metal vias. The classical metal plasticity model in the ABAQUS is adopted for the via material, with rate-independent perfect plasticity and a von-Mises yield surface for associated plastic flow [77]. In general, the rate-independent model is used to simulate metals deformed at relatively low temperatures (less than half of the material's melting point) and modest strain rates (of order 0.01-10/s). In the metal plasticity, the total strain can be decomposed into elastic and plastic parts. A yield surface, f, is defined as the limit of the elastic response. Inside the yield surface ($f < 0$), the corresponding stress state is linear elastic. During plastic flow, $f = 0$ (and $df = 0$), and no strain hardening is considered.

For the yield criteria, the von-Mises stress or equivalent shear stress (σ_{eq}) is used, which is related to the deviatoric stress as

$$\sigma_{eq} = \sqrt{\frac{3}{2} s_{ij} s_{ij}} , \tag{2.11}$$

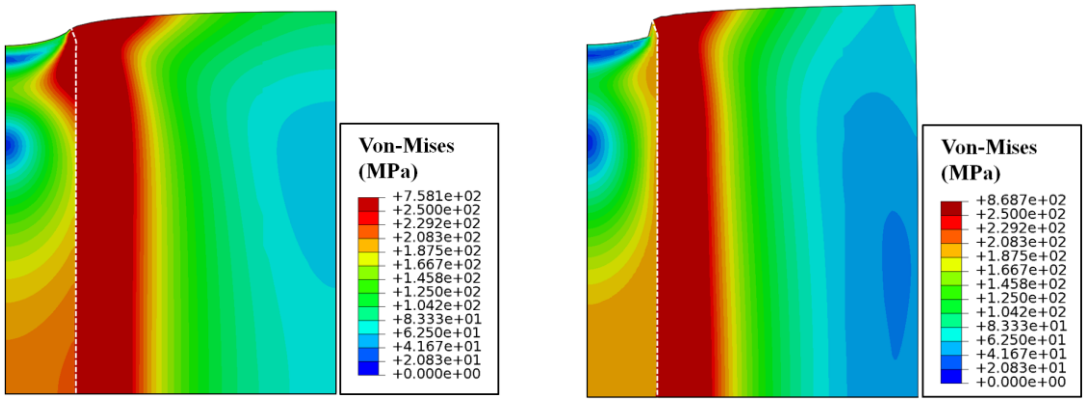
where $s_{ij} = \sigma_{ij} - \frac{1}{3}\sigma_{kk}\delta_{ij}$. Similarly, the equivalent plastic strain (or the equivalent von-Mises strain, ε_{eq}) is used to represent the effective plastic flow, namely

$$\varepsilon_{eq} = \sqrt{\frac{3}{2} e_{ij} e_{ij}}\ , \tag{2.12}$$

where $e_{ij} = \varepsilon_{ij} - \frac{1}{3}\varepsilon_{kk}\delta_{ij}$.

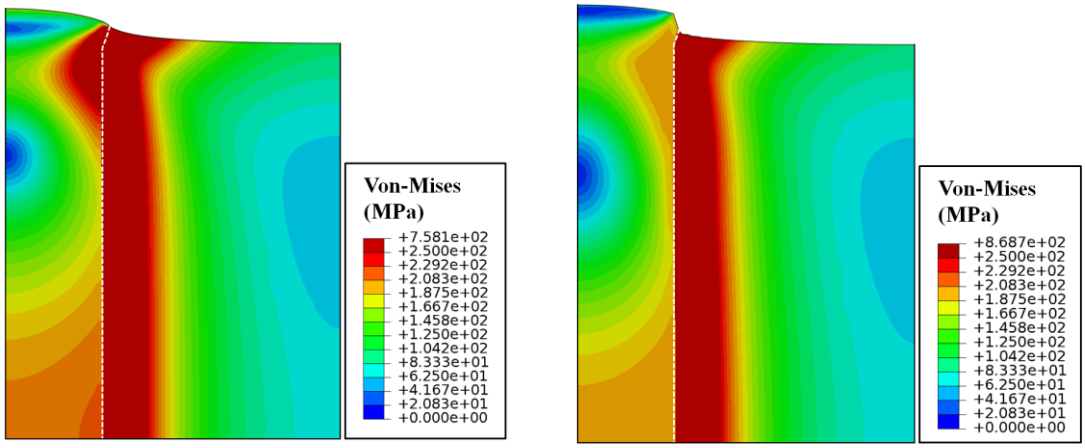
The yield strength for the Cu via is taken to be $\sigma_y = 200$ MPa based on previous studies for electroplated Cu films with similar grain sizes [78-80]. In practice, the yield strength would be dependent of temperature, but it is assumed independent of temperature in this study. In the calculation, a TSV structure with $D_f = 30\,\mu\text{m}$ is considered with the thermal loads, $\Delta T = \pm 250\,^{o}\text{C}$. For comparison, the deformed shapes as well as the von-Mises stresses are shown in Figure 2.8 for an elastic model and the plastic model for the same thermal loads. As shown, the maximum von-Mises stress in the via for the elastic model exceeds the given yield strength (200 MPa). In the plastic model, due to plastic yielding of the via material, the maximum von-Mises stress in the via equals the yield strength. It is noted that the plastic deformation is largely confined in a small volume near the junction between the via/Si interface and the wafer surface, as shown by the contours of the equivalent plastic strain in Fig. 2.9. As a result, the stress distributions in Si around the via are similar in both models. On the other hand, the deformed shapes by the plastic model are considerably different from the elastic model, especially at the locations near the wafer surface. Under the negative thermal load ($\Delta T = -250\,^{o}\text{C}$), the via surface in the elastic model is deformed in a smooth concaved shape. However, in the plastic model, the via surface sinks in abruptly near the interface due to local plastic yielding. Meanwhile, via extrusion is predicted for the positive thermal load ($\Delta T = 250\,^{o}\text{C}$), which is enhanced by the local plastic deformation in the via. Here, the via/Si interface is assumed to be intact. As will be discussed in Chapter 4,

via extrusion could also be enhanced by interfacial delamination. The phenomenon of via extrusion has been observed as a common failure mode for TSV structures (Fig. 1.11c). Moreover, as will be discussed in Chapter 3, the material plasticity and via extrusion are also observed in the bending beam experiments subjected to thermal cycling.



(i) The elastic model (ii) The plastic model

(a)



(i) The elastic model (ii) The plastic model

(b)

Figure 2.8: Comparison of stress distribution and deformation between an elastic and a plastic model with different thermal loads ($D_f = 30\,\mu\text{m}$): (a) Thermal load, $\Delta T = -250\,^{\circ}\text{C}$; (b) Thermal load, $\Delta T = 250\,^{\circ}\text{C}$.

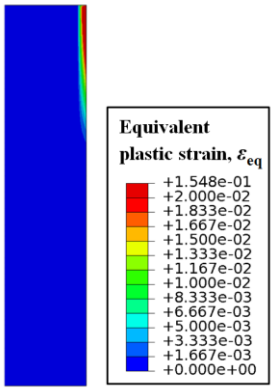


Figure 2.9: Equivalent plastic strain in the via by the plastic model ($D_f = 30\,\mu\text{m}$ and $\Delta T = 250^{\circ}\text{C}$).

2.5 SUMMARY

In this Chapter, the characteristics of thermal stresses in a TSV structure were analyzed by a semi-analytical approach and FEA calculations. The main focus was on the stress distributions near the wafer surface, where most electronic devices are located. The effect of wafer thickness was discussed. The anisotropic elastic properties of silicon resulted in an anisotropic stress distribution around the via. The effects of plasticity in the via were investigated for both positive and negative thermal loads. The results in this chapter provide a baseline understanding of the thermomechanical stresses in the TSV structures, which will be compared with the experimental measurements in Chapter 3 and then used in the study of interfacial reliability in Chapter 4.

Chapter 3

Stress Measurements for TSV Structures

As discussed in Chapter 1, processing-induced thermal stresses could be sufficiently high to cause failure of the integrated TSV structures, and the stresses in Si around TSVs may degrade the performance of transistors through the piezoresistivity effect. Thus, in addition to numerical analysis, it is essential to experimentally measure and characterize the stresses in the TSV structures. In this Chapter, two experimental methods are developed to measure the thermal stresses in the TSV structures: Bending beam technique and micro-Raman spectroscopy. The experimental results are compared to numerical simulations.

3.1 Bending Beam Technique

The bending beam (BB) technique is similar to the wafer curvature method for characterizing stresses in thin films [76]. Typically, Stoney's formula is used to determine the average stress in a thin film based on the measurement of wafer curvature. The method has been extended to measure volume average stresses in periodic Al and Cu line structures subjected to thermal load [81-83]. For the TSV structures, the bending beam technique allows measurement of the curvature and average stress during thermal cycling, based on which the elastic and plastic behavior can be deduced. However, unlike thin films, the classical Stoney's formula does not apply for the TSV structures to directly convert substrate curvature into stresses, due to the three-dimensional stress distribution in the TSVs as discussed in Chapter 2. In the present study, finite element analysis (FEA) was performed to determine the stress distribution and to examine the effect of plasticity.

3.1.1 The Bending beam system

The system for the bending beam measurements employs an optical method to monitor the curvature change of the specimen during thermal cycling. Figure 3.1 shows a schematic setup of the system used for this research.

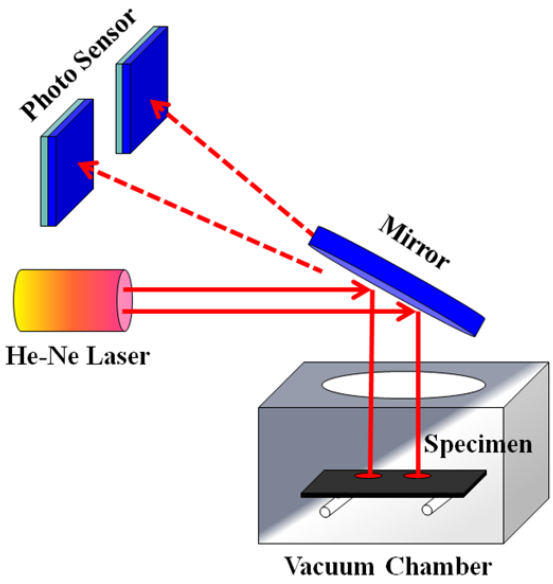
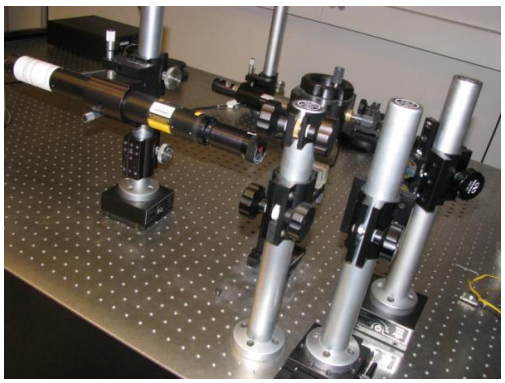
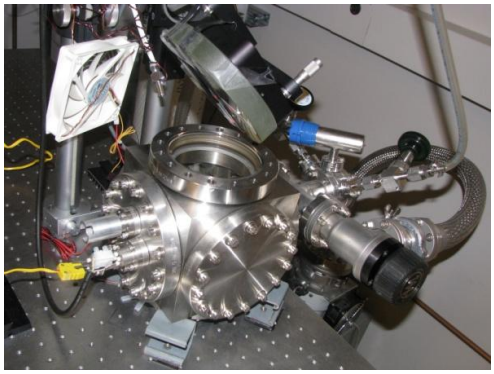


Figure 3.1: Illustration of the bending beam system.

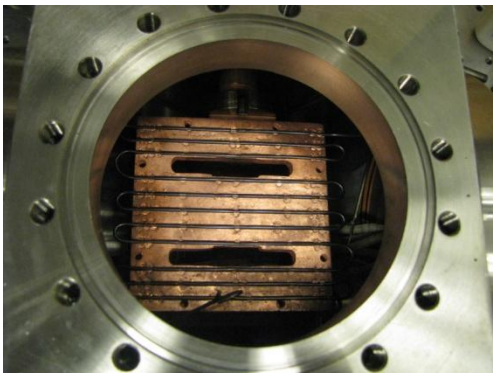
The system consists of (a) a He-Ne laser, (b) a vacuum chamber, (c) a heating plate, (d) a temperature controller, (e) photo detectors, and (f) a laser-positioning system, as shown in Fig. 3.2. The heating plate is installed above the specimen and the heating rate of the sample is controlled by the temperature controller. The system does not have a cooling system, and thus the cooling rate is dictated by the natural cooling rate of the system.



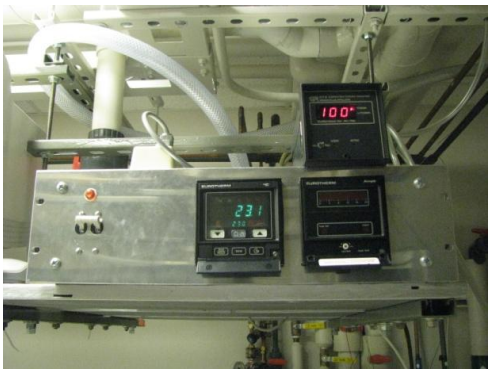
(a) The He-Ne Laser System



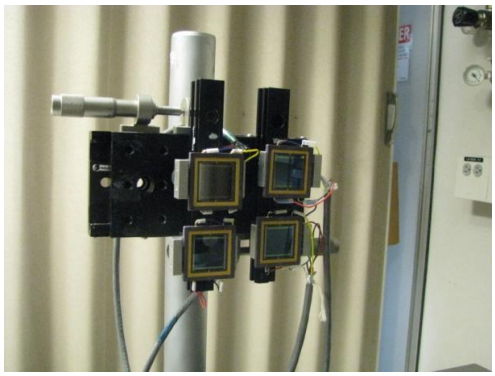
(b) The Vacuum Chamber



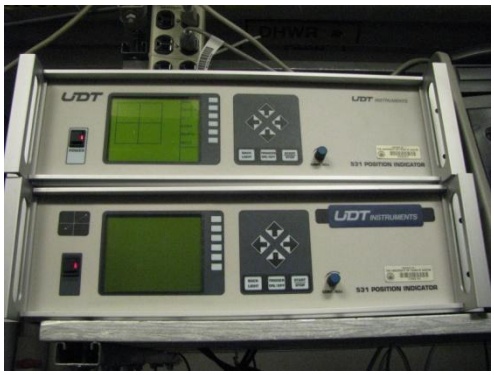
(c) The Heating Plate



(d) The Temperature Controller



(e) The Photo Detectors



(f) The Positioning System

Figure 3.2: Key components of the bending beam system.

In the bending beam system, the two parallel He-Ne laser beams are directed to certain locations on the surface of the specimen (blue dashed line in Fig. 3.3), and then reflected onto the two photo detectors. The specimen is typically placed in a nitrogen atmosphere to prevent oxidation. A base pressure of 100 torr is maintained in the vacuum chamber during the tests. As the temperature changes, the specimen deforms (blue solid line in Fig. 3.3) and as a result the positions of the reflected lasers (red dash lines in Fig. 3.3) changes from their original locations (red solid line in Fig. 3.3). The laser-positioning system tracks the traces of the two laser beams during thermal cycling by recording the x (lateral) and y (vertical) coordinates of the laser locations. In this way, the distance between the two laser spots on the photo sensors, S, is obtained and used for the curvature calculation. In addition, the specimen often has an initial curvature, which has to be subtracted from the measured curvature to obtain the curvature change due to thermal loading in the bending beam experiment. Finally, the curvature change during thermal cycling can be deduced as following:

$$\kappa - \kappa_o = \frac{1}{R} - \frac{1}{R_o} = \frac{S_o - S}{2LM}, \tag{3.1}$$

where R is the radius of curvature, L is the distance between two laser spots on the specimen (L = 2.75 cm), and M is the distance between the specimen and the photo sensors (M = 2.248 m). M is assumed to be constant, neglecting the small change due to deformation of the specimen. The subscript "o" stands for the baseline values at the reference (initial) state.

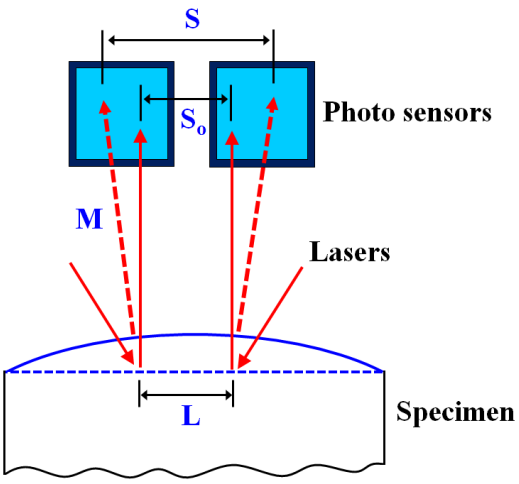


Figure 3.3: Spatial relationships for the curvature calculation of the specimen.

For a thin film specimen, the measured curvature can be directly converted to the average stress in the thin film using the Stoney's equation [76]:

$$\sigma_f = \frac{E_s t_s^2}{6(1-\nu_s)t_f}\left(\frac{1}{R}-\frac{1}{R_0}\right), \tag{3.2}$$

where σ_f is the average stress (assumed to be equi-biaxial) in the film, E_s and ν_s are the Young's modulus and Poisson's ratio of the substrate, and t_s, t_f are the thicknesses of the substrate and film, respectively. For a TSV specimen as described in the next section, however, the Stoney's equation cannot be used due to the complexity of stress distribution in the specimen. Therefore, finite element method (FEM) was applied in this research for stress analysis.

3.1.2 TSV specimen and curvature

The TSV specimen used in this study consisted of periodic arrays of blind Cu vias with 10 μm diameter (D_f) and 55 μm depth, as shown schematically in Fig. 3.4. The

pitch distances are 50 μm and 40 μm in the longitudinal and transverse directions, respectively. As received, the top surface of Si was covered with an oxide layer of 0.8 μm thick. An oxide barrier layer of about 0.4 μm thick was deposited at the via/Si interface. The specimen was 5 mm wide, 50 mm long, and 700 μm thick. The TSV arrays were arranged in parallel patterns along the center line of the specimen (~600 μm wide).

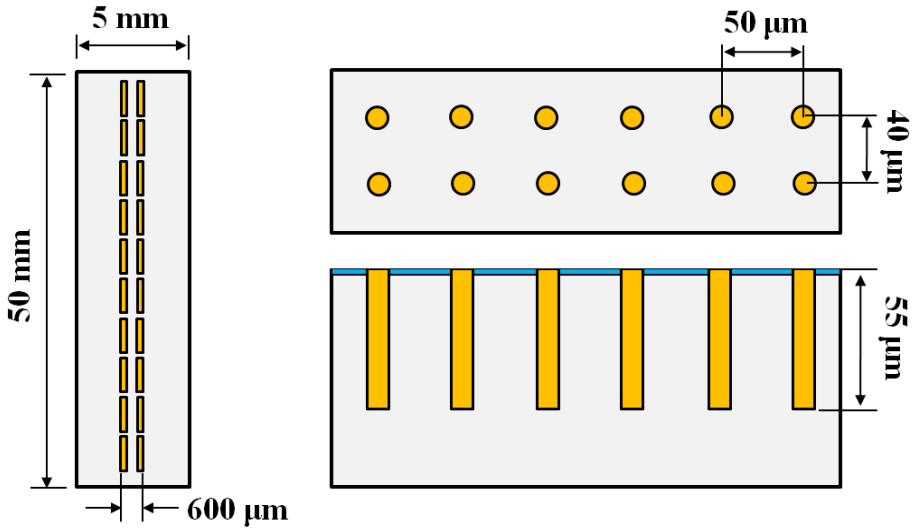
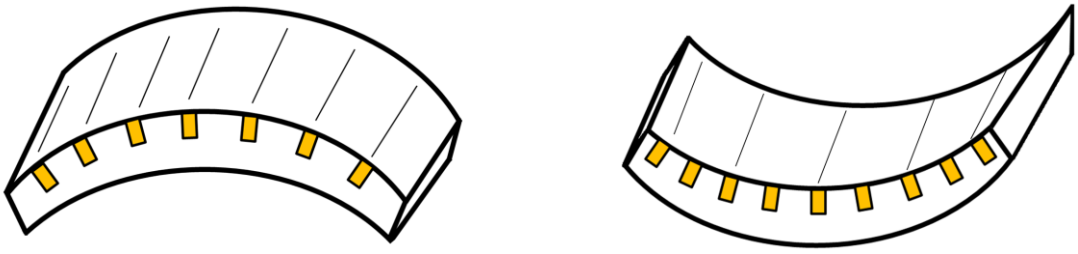


Figure 3.4: Illustration of the TSV specimen for bending beam experiment.

To facilitate the discussion of the experimental results, the sign convention for the curvature of the TSV specimen is illustrated in Fig. 3.5. In general, because Cu has larger CTE than the other materials (oxide and Si), a positive thermal load ($\Delta T > 0$) causes the upper part of the specimen where the TSVs are located to expand more, generating the deformation shape shown in Fig. 3.5a. In the present study, such a curvature is defined as 'negative'. If the specimen bends the opposite way, which is the case for a negative thermal load ($\Delta T < 0$), the curvature is referred to as 'positive'. It should be noted that

only the average curvature along the longitudinal direction of the specimen is measured in the bending beam test.



(a) (b)

Figure 3.5: Sign definition of the beam curvature in the experiment: (a) A negative curvature; (b) A positive curvature.

3.1.3 Bending beam experiments

Experimental procedure

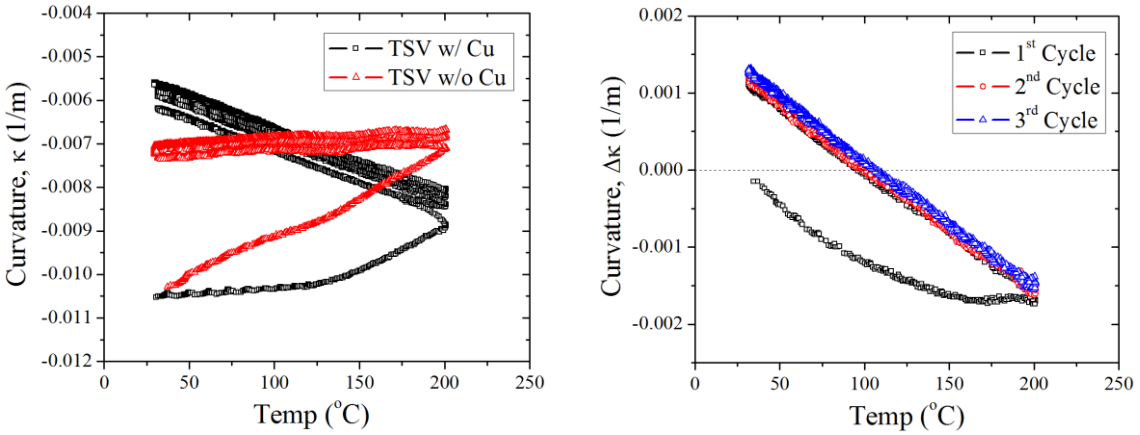
The procedure for the bending beam experiment is described in details as the following. First, the TSV specimen is placed into the vacuum chamber, and the stability of the sample is checked. Next, the position of the photo sensors or the placement of the sample is adjusted to ensure that the reflected laser beams properly fall onto the photo sensors. Upon completing the alignment of the photo sensors and the specimen, the heating plate is installed above the specimen and electrically connected to the external temperature controller. After completing all set-up for the sample, the oxygen remaining inside the vacuum chamber is pumped out by a vacuum pump till the indicator shows 0~2 mtorr, to protect materials from oxidation during thermal cycling. Then, nitrogen gas to form a protection atmosphere is charged into the vacuum chamber till the pressure becomes 100 torr. After the pressure inside the vacuum chamber has stabilized, the heater is turned on, and a customized LabVIEW program is executed for data collection.

Initial curvature

During sample preparation, an initial curvature is typically developed due to process-induced residual stresses. To evaluate thermal stresses in the TSVs during thermal cycling, two specimens were used, one of which serves as the reference with the Cu vias etched off using nitric acid. Both specimens were heated to 200^{o}C with a heating rate of 2^{o}C/min, followed by cooling back to the room temperature (~30^{o}C). As shown in Fig. 3.6a, the curvature changed significantly during the first heating for both specimens, which is also commonly observed for thin film specimens. Subsequently, the curvature changes almost linearly with temperature for several cycles. Interestingly, the curvature/temperature slopes for the two specimens have different signs, negative for the specimen with Cu vias and positive for the specimen without Cu. The curvature difference between the two specimens is attributed to the thermal stress in the Cu vias, as plotted in Fig. 3.6b. During the first cycle, the curvature decreases nonlinearly as the temperature increases, suggesting an average compressive stress in the Cu vias and inelastic deformation possibly due to evolution of Cu grain structures. During subsequent cycles, however, the curvature-temperature relation is nearly linear and reversible, indicating an elastic behavior with negligible effect of plasticity in Cu. This behavior is in sharp contrast with wafer curvature measurements of Cu thin films, which is typically nonlinear with a hysteresis loop due to plasticity [82, 84]. The difference can be partly attributed to the triaxial stress states in the Cu vias. In this cae, the effects of geometry and confinement may play an important role in suppressing plasticity in the Cu vias. As discussed later in Section 2.4, plastic deformation is confined within a small volume, and the effect may not be observable from the curvature measurement.

It is noted that, after the first cycle, the curvature difference between the two specimens becomes zero at around 100^{o}C, which is consistent with the annealing

temperature after Cu electroplating of the TSV structure. It may be assumed that the stresses in the Cu vias are largely relaxed during annealing when they were fabricated, i.e. the stresses in Cu vias can be assumed to be zero at 100 °C. The temperature 100°C is then used as the reference temperature for calculating thermal stresses in the TSV structures by finite element analysis.



(a) (b)

Figure 3.6: Comparison of bending beam measurements of two TSV specimens, with and without Cu vias. (a) Raw data from the bending beam tests; (b) Curvature difference between the two specimens.

Effect of maximum thermal loading

In this section, the effect of maximum thermal loading applied during thermal cycling was investigated. For this study, the oxide layer on the surface of the TSV specimen was mechanically polished off. The specimen was then subjected to four thermal cycles, as shown in Fig. 3.7.

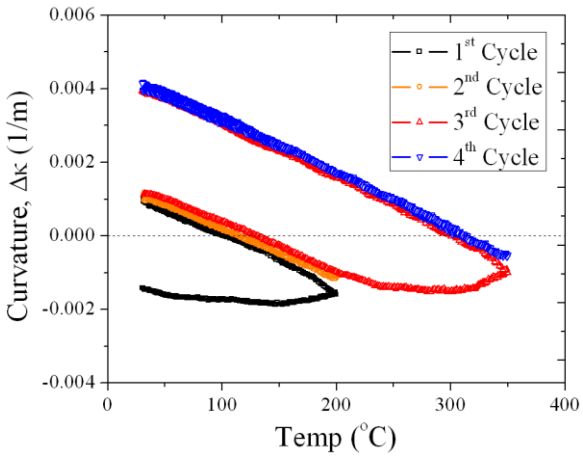


Figure 3.7: Bending beam measurement of a TSV specimen with the surface oxide polished off.

In the first two cycles, the specimen was heated to 200°C, and the curvature behavior is similar to that in Fig. 3.6b for the specimen with the surface oxide layer. During the third and fourth thermal cycles, the specimen was heated to 350°C. As the specimen was heated beyond 200°C in the third cycle, the curvature-temperature relation becomes nonlinear, indicating inelastic stress relaxation at higher temperatures [82, 85, 86]. The mechanism of such stress relaxation is not fully understood. Similar to Cu thin films, inelastic deformation at high temperatures may be attributed to dislocation plasticity and diffusional creep [87]. However, the triaxial stress state in TSVs would reduce the extent of plasticity and its contribution to the inelastic deformation. Instead, we observed significant grain growth in the Cu vias from 200°C to 350°C by focused-ion beam (FIB) images, which will be discussed further in Section 3.1.4. In principle, the grain growth process would also reduce the thermal stress in the Cu vias [88]. Subsequently, in the fourth cycle, the curvature-temperature again becomes nearly linear between room temperature and 350°C, suggesting that the grain structure has been

stabilized up to 350°C. Further increasing the temperature would expect to result in more grain growth and stress relaxation.

To further study the effect of the maximum thermal loading, bending beam tests were performed using two other specimens as shown in Fig. 3.8. The first specimen underwent thermal load to 350°C in the third cycle, followed by another cycle to 400°C as shown in Fig. 3.8a, whereas the second specimen was directly heated up to 400°C in the third cycle as shown in Fig. 3.8b. Apparently, more inelastic deformation is observed as the first specimen was heated beyond 350°C in the fourth cycle. Interestingly, the final curvatures are similar for the two specimens after four thermal cycles. Thus, the amounts of grain growth and stress relaxation are similar in both specimens, despite slightly different thermal cycles. In particular, the maximum temperature during all thermal cycles is believed to play a critical role in stabilizing the grain structures in the Cu vias.

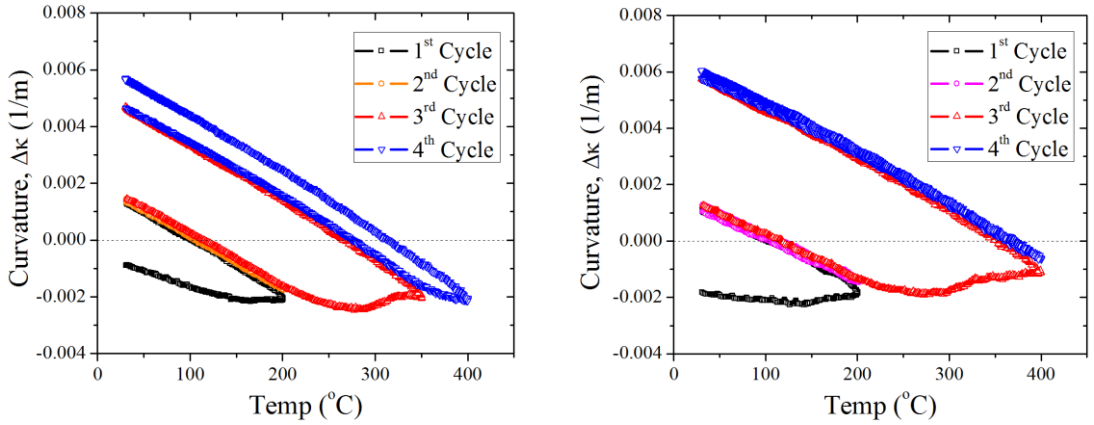
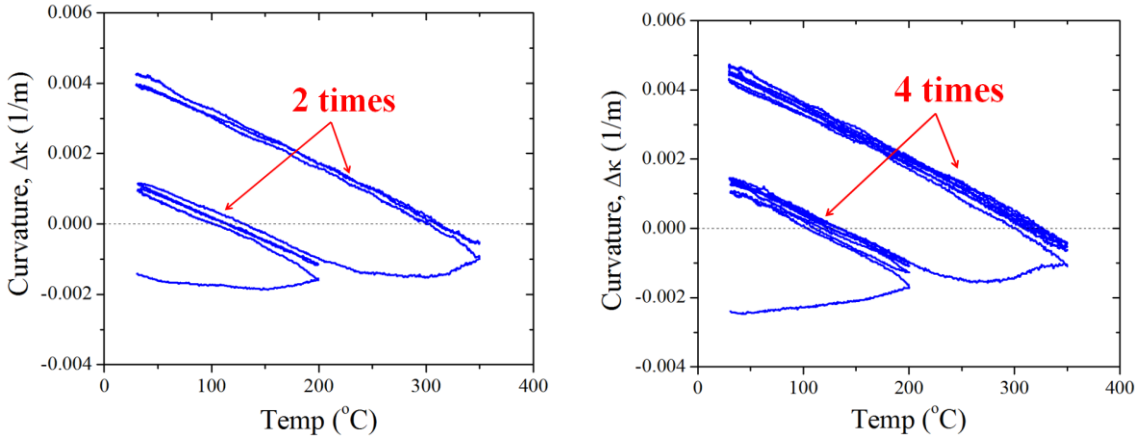


Figure 3.8: Effect of maximum thermal load on BB results: (a) Thermal cycling to 400°C after 350°C; (b) Thermal cycling to 400°C.

Effect of the number of thermal cycles

It was found that the curvature-temperature curve in the bending beam test shifts as the number of thermal cycles increases. As shown in Fig. 3.9a, the TSV specimen first underwent two cycles up to 200°C and then two more cycles to 350°C. For comparison, in Fig. 3.9b, the specimen underwent four cycles to 200°C and then four cycles to 350°C. The overall behavior is very similar in both tests. However, in Fig. 3.9b, with repeated thermal cycling to the same temperature (200°C and 350°C), a slight upward shift of the curvature was observed. This curvature shift indicates slightly inelastic behavior during the thermal cycles, despite that the grain structures of the Cu via are largely stabilized. The observed curvature shift behavior is similar to thermal ratcheting, which may result from localized plastic deformation in the vias. Alternatively, the inelastic behavior may be attributed to continual evolution of the grain structures of the Cu vias over the thermal cycles. Although the amount of grain growth may be relatively small each cycle, the change of the grain structures becomes observable over increasing number of cycles, as will be shown by the microstructure analysis in the next section.



(a) (b)

Figure 3.9: Effect of the number of thermal cycles on BB results: (a) 2 times cycling; (b) 4 times cycling.

3.1.4 Microstructure analysis[1]

To evaluate the effect of the Cu microstructures on the stresses in TSVs, a series of bending beam experiments were performed, with one thermal cycling for each sample. The maximum temperature is varied from 100 °C to 400°C as shown in Fig. 3.10. After each bending beam test, the focused ion beam (FIB) method [89] was performed to examine the grain structure in the Cu via. For all the tests, the curvature-temperature behavior is nonlinear during heating and almost linear with nearly identical slope during cooling.

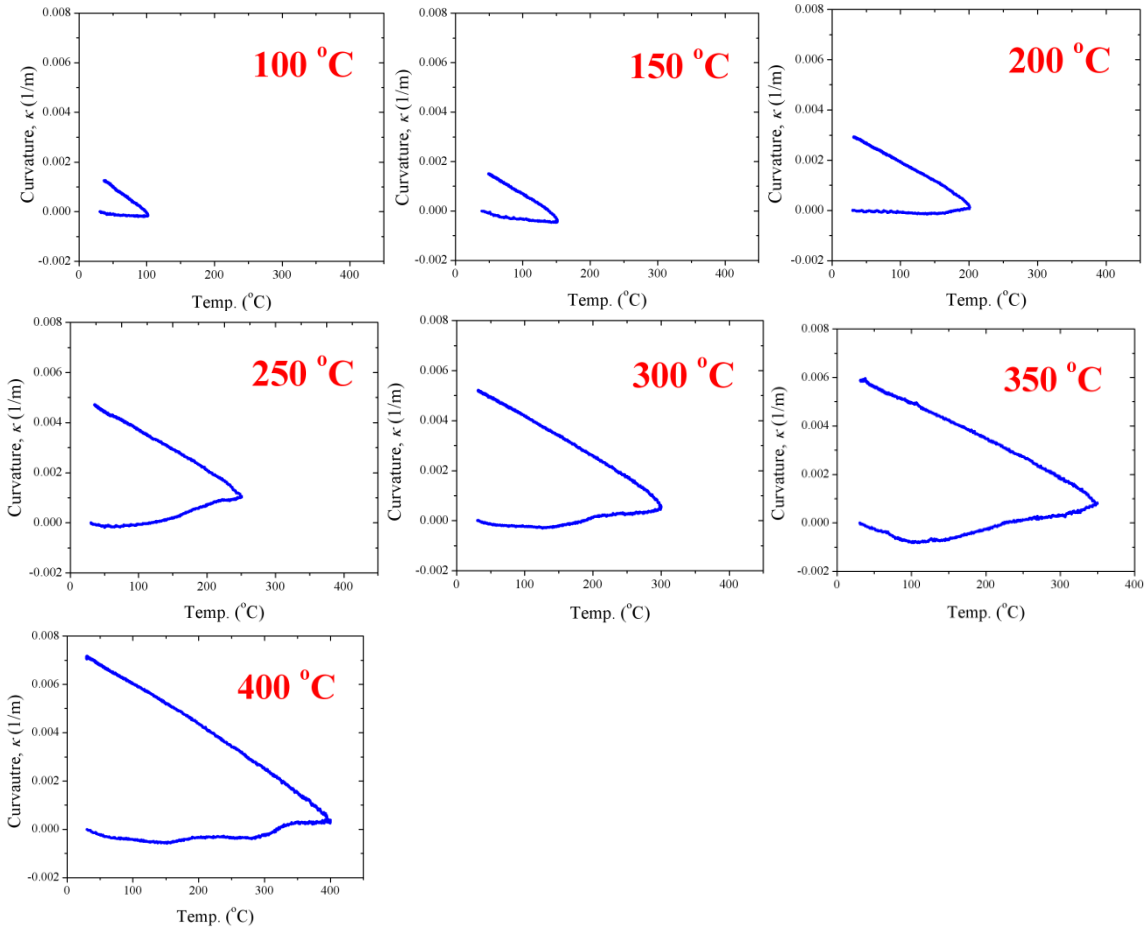


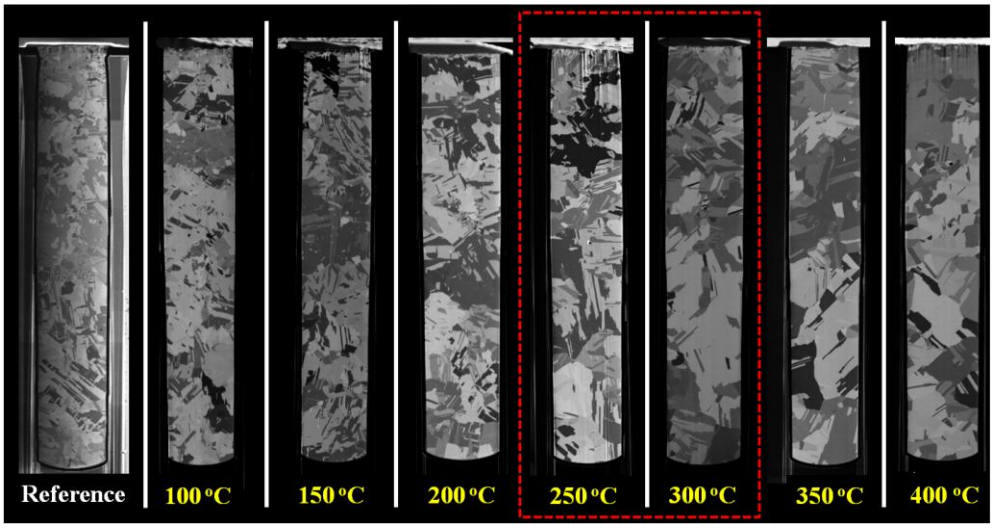
Figure 3.10: Bending beam results for different thermal loads.

[1] *In collaboration with Tengfei Jiang, The University of Texas at Austin*

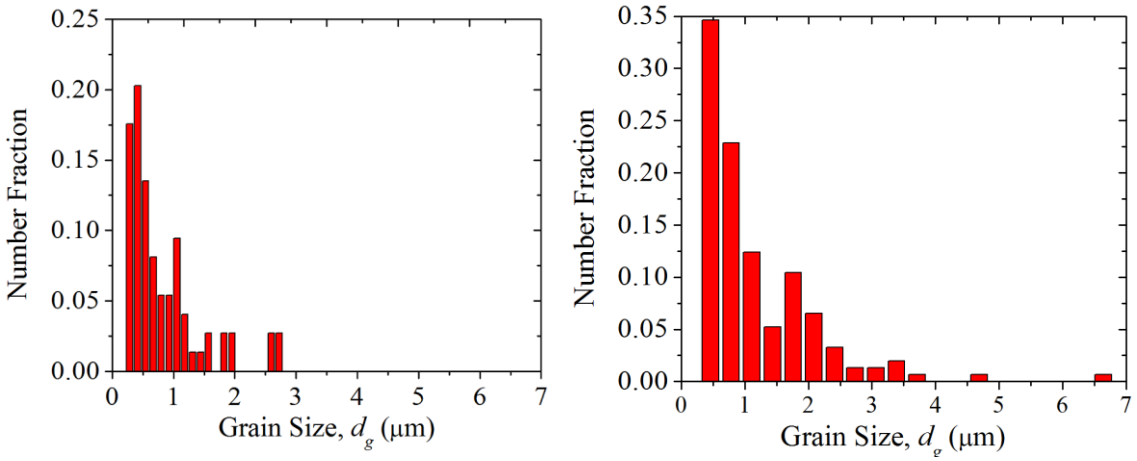
Figure 3.11a shows the FIB images. Due to the ion channeling effect, grains with different orientations show different contrast in the FIB images, therefore allowing qualitative analysis of the grain structure. Without thermal cycling, the grain size in a reference sample increases from the top of the via to the bottom. Near the surface of the via, very small grains exist, while the bottom of the via has relatively large grains. This observation is consistent with that reported in other studies [90, 91]. During the electroplating of TSVs, the grain growth is mostly determined by the additive concentration since the additives hinder the grain boundary motion and segregate at the grain boundaries to reduce grain boundary energy [92]. Usually, the top of the TSV has higher concentration of additives than the bottom of the TSV due to the difference in the flow rate of electrolyte and current density during electroplating. Therefore, the observed grain structure is characteristic for the electroplated TSVs.

After thermal cycling, as shown in Fig. 3.11a, the Cu grain sizes in the vias increase with increasing thermal loads. Especially, a large transition in the grain size is observed from 250^{o}C to 300^{o}C (in a red dash box). For the reference sample and the sample which was thermally cycled to 350^{o}C, the grain sizes and orientations were measured by electron backscattering diffraction (EBSD). The bar graphs in Fig. 3.11b plot the grain size distribution for the two samples. The average grain sizes for the reference and the 350^{o}C-annealed sample were 0.71 μm and 1.18 μm, respectively. Overall, the grain size after 350^{o}C thermal cycling grew around 66% when compared to the reference sample. From the EBSD, no preferred grain orientation was observed in either sample. Furthermore, a large number of twin boundaries were observed with a characteristic 60^{o} misorientation angle across the boundaries. The percentages of twin boundaries are similar for both samples. The presence of these twin boundaries may play

an important role in the mechanical behavior of the Cu vias, especially for the mechanisms of dislocation plasticity and grain boundary diffusion.



(a)

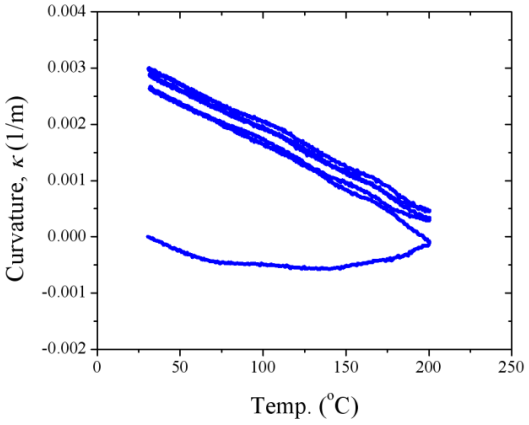


(i) reference sample (ii) after thermal cycling to 350 °C

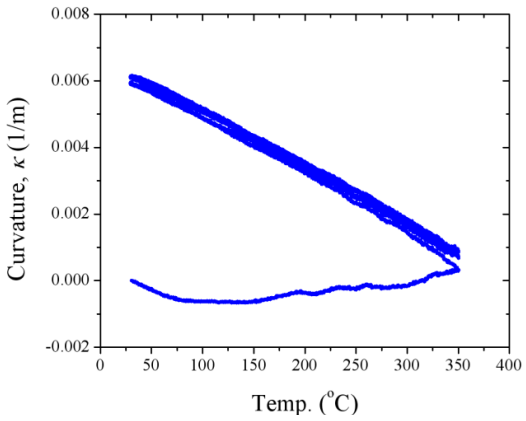
(b)

Figure 3.11: Analyses of Cu grain sizes in TSVs before and after thermal cycling: (a) FIB images of the Cu grain structures; (b) Grain size distributions by EBSD analysis.

In addition, BB experiments were performed with three thermal cycles to 200 °C and 350°C for two specimens, respectively, as shown in Fig. 3.12a. FIB images of the Cu vias in these samples are compared to those after only one thermal cycle to the same temperatures in Fig. 3.12b. Qualitatively speaking, slight grain growth has occurred.

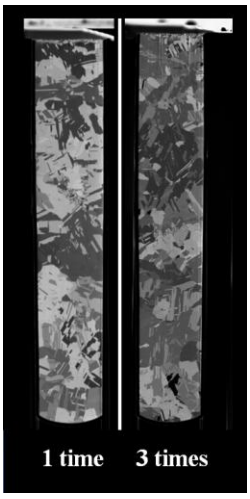


(i) T_{max} = 200°C

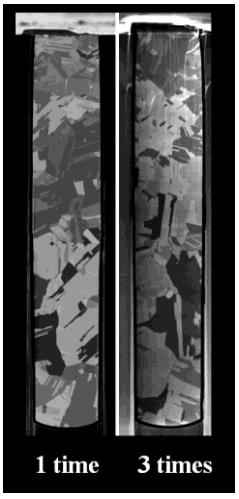


(ii) T_{max} = 350°C

(a)



(i) 200°C



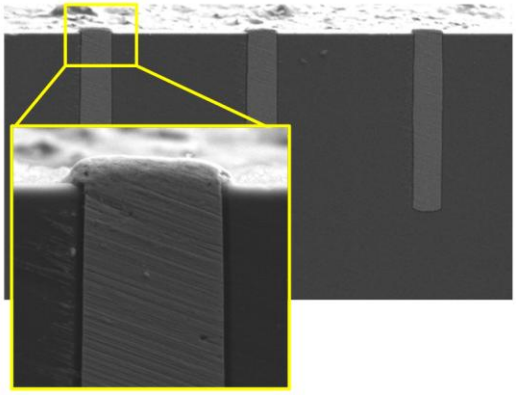
(ii) 350°C

(b)

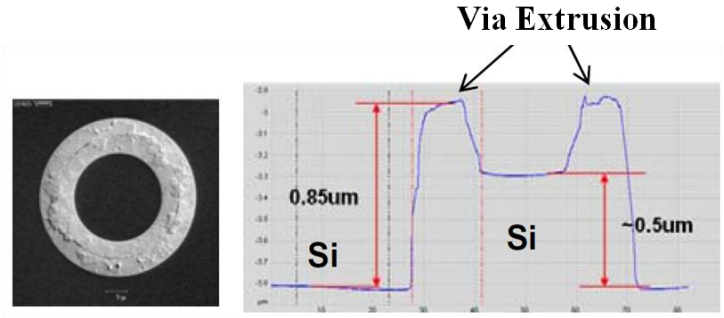
Figure 3.12: Effect of multiple thermal cycling on grain size: (a) Bending beam results with three thermal cycles; (b) Comparison of grain structures after one and three thermal cycles.

3.1.5 Via extrusion

After subjected to the thermal cycling, the TSV specimen was cross-sectioned for scanning electron microscope (SEM) imaging. As shown in Fig. 3.13, extrusion of Cu vias is evident. Theoretically via extrusion may result from two possible mechanisms. First, as shown in Fig. 2.8, local plastic deformation in the via could lead to via extrusion. Second, as will be discussed in Chapter 4, interfacial delamination between the via and Si could also lead to via extrusion. From the SEM image in Fig. 3.13, no evidence of interfacial delamination was observed. Thus, the observed via extrusion may be attributed to the local plastic deformation in the Cu vias. Similar via extrusion was observed for an annular TSV as shown in Fig. 3.13b.



(a)



(b)

Figure 3.13: TSV extrusion: (a) SEM image after thermal cycling; (b) Via extrusion of annular TSV (Source: Samsung [53]).

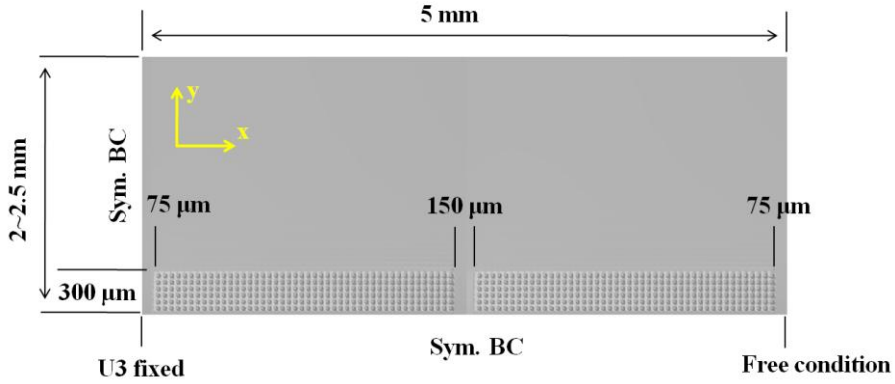
3.1.6 Finite element analysis

The curvature measured in the bending beam tests can be converted to volume average stresses in the TSVs, similar to the wafer curvature tests for periodic line structures [81, 83, 93-96]. However, the specimens used in the present study contained TSVs only in a narrow region along the center line, for which the volume average approach becomes less effective. Instead, finite element analysis (FEA) was performed to determine the deformation and stress distribution in the TSV specimen. Figure 3.14a shows the FEA model, with symmetric boundary conditions for the left and lower sides. To reduce the computational cost, only a quarter of the specimen is modeled. All the materials are assumed to be linear elastic for the moment, with the properties listed in Table 3.1.

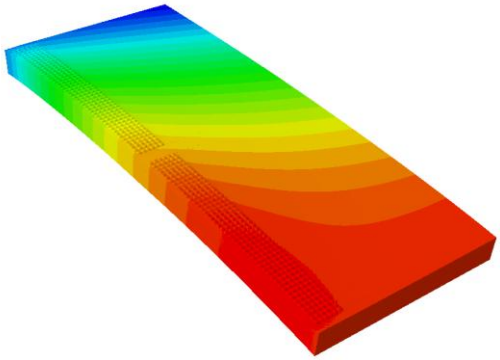
Table 3.1: Thermomechanical properties used in finite element analysis.

Material	CTE (ppm/^{o}C)	Young's Modulus (GPa)	Poisson's ratio
Cu	17	110	0.35
Si	2.3	130	0.28
Oxide	0.55	72	0.16

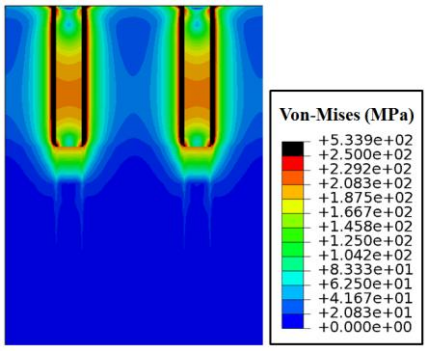
As shown in the FEA results, the specimen bends non-uniformly due to mismatch in thermal expansion (Fig. 3.14b). An average curvature is determined along the center line of the specimen, and the rate of curvature change, $\Delta\kappa/\Delta T$, is calculated for comparison with the bending beam tests. As shown in Fig. 3.7, the experimentally measured curvature change is nearly linear with respect to the temperature during cooling in all cycles as well as heating in the second and fourth cycles; the rate of curvature change in the linear region is approximately -1.47E-5 $m^{-1}/^{o}C$. The FEA calculated rate of curvature change is -1.88E-5 $m^{-1}/^{o}C$, in fair agreement with the BB measurements.



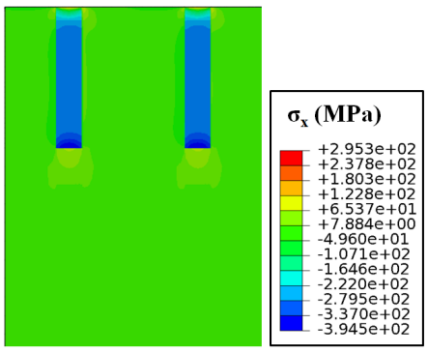
(a)



(b)



(c)



(d)

Figure 3.14: FEA results for $\Delta T = 200\,^{o}\mathrm{C}$: (a) 3D FEA Model; (b) Deformed shape upon heating; (c) Von-Mises stress; (d) Lateral stress.

Figure 3.14 c-d show the stress distribution in the TSV structure, corresponding to an average curvature, $\kappa = -3.76\text{E}-3$ m^{-1}. The magnitude of stress is proportional to the average curvature in the linear model. Therefore, it is possible to convert the measured curvature from the bending beam tests to stress distributions by scaling the stress magnitude proportionally. In particular, the maximum von-Mises stress in the Cu vias is critical for understanding the effect of Cu plasticity. By the elastic FEA model, the maximum von-Mises stress in the via is found to be about 325 MPa at the curvature $\kappa = -3.76\text{E}-3$ m^{-1}. Assuming a linear relation between the stress and the curvature, the measured curvature-temperature curves in Fig. 3.7 are converted to stress-temperature curves for volume-averaged lateral stress in Fig. 3.15.

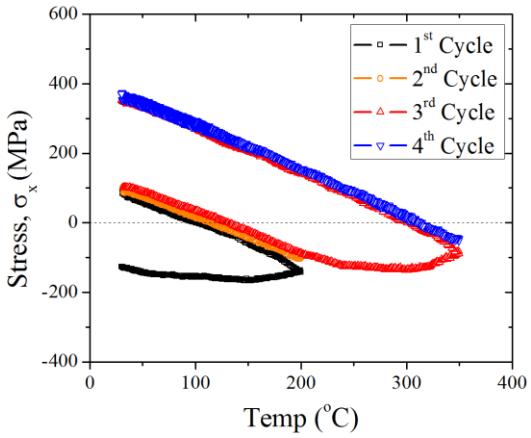
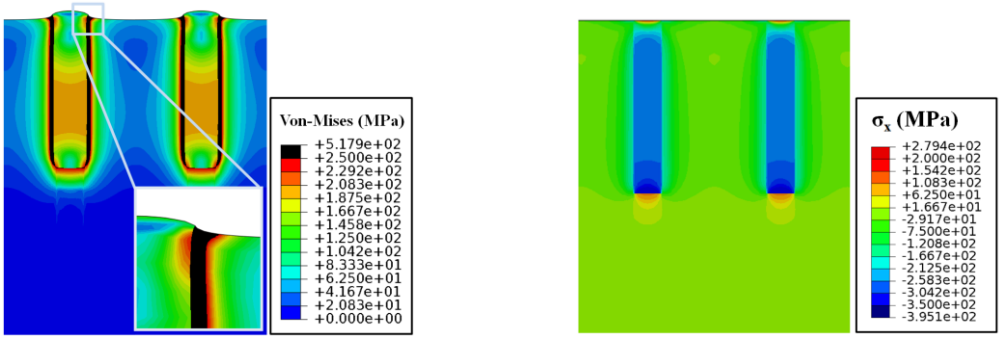


Figure 3.15: Stress-temperature curve based on a linear relation between stress and curvature.

As discussed previously, plastic deformation and grain growth in the Cu vias could lead to stress relaxation and Cu extrusion during thermal cycling. Assuming an elastic-plastic behavior for the Cu vias with the yield strength of 250 MPa, we calculated the deformation and stress distribution in the Cu vias, as shown in Fig. 3.16. In practice, the yield strength could be different since the yield strength depends on temperature and

grain size. It is noted that the von-Mises stress as the effective shear stress for plastic deformation is non-uniform in the Cu vias, which reaches the yield strength in a small region near the junction between the via/Si interface and the upper surface. As a result, the plastic deformation in the Cu vias is highly localized, in contrast to Cu thin films where the stress is nearly uniform and plastic deformation occurs over the entire film volume. While the local plastic deformation is sufficient to cause via extrusion, it does not seem to have much effect on the overall curvature of the specimen, which explains why no hysteresis loop was observed in the bending beam tests. On the other hand, during the first cycle and the third cycle of the bending beam test shown in Fig. 3.7, the nonlinear curvature-temperature behavior suggests significant stress relaxation induced by grain growth. The grain growth could lead to lower yield strength of the Cu vias by the Hall-Petch effect [79, 97], which in turn leads to more extensive plastic deformation and Cu extrusion. Thus it is important to stabilize the grain structures of the Cu vias before subsequent processes in order to minimize via extrusion. This may be achieved by high-temperature annealing as observed in the FIB images.

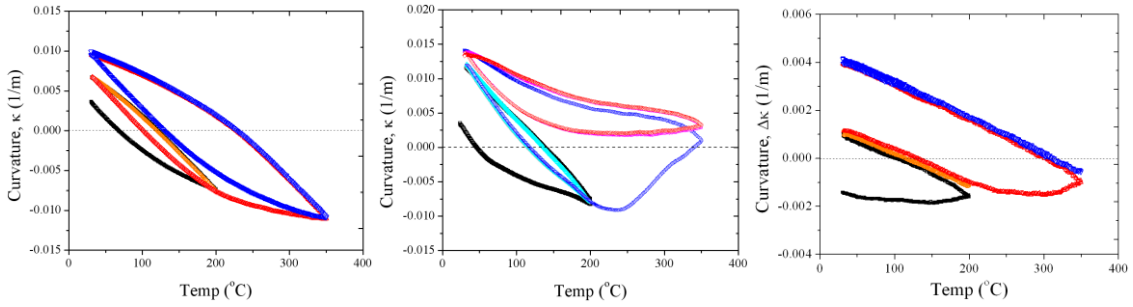


(a) (b)

Figure 3.16: Plastic FEA results for $\Delta T = 200\,^{o}\mathrm{C}$ with yield strength, $\sigma_y = 250\,\mathrm{MPa}$: (a) Von-Mises stress; (b) Lateral stress.

3.1.7 Comparison of BB behaviors among different TSV structures

For comparison, bending beam experiments were conducted with a thin film specimen and an annular TSV specimen. The thin film specimen consists of an electroplated Cu film of 0.6 μm thick on a 300 μm Si substrate. The annular TSV specimen consists of an array of annular Cu vias in a 700 μm thick wafer. The via diameter is 90 μm, with 1.6 μm thick Cu layer, and the via-to-via pitch distance is 360 μm. As shown in Fig. 3.17, the three structures have distinctly different BB behaviors.

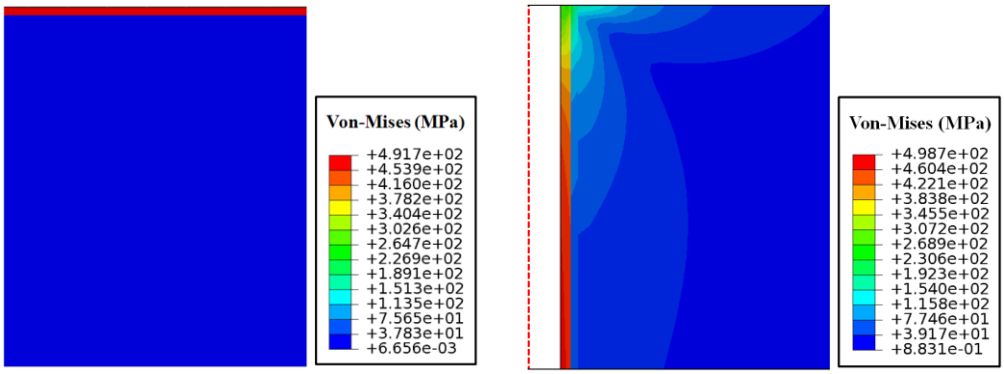


(a) (b) (c)

Figure 3.17: Comparison of BB behaviors among different structures: (a) Thin film; (b) Annular TSV; (c) Fully-filled TSV.

The thin film specimen exhibits a typical hysteresis loop during thermal cycling. In contrast, the fully-filled TSV, which shows large stress relaxation during the first cycle, does not have the hysteresis loop in the subsequent cycles, as discussed in the previous sections. The behavior of the annular TSV specimen seems to combine the characteristics of both the thin film and fully-filled TSV: it has a hysteresis loop similar to that of the thin film, but with significant stress relaxation at high temperatures similarly to the fully-filled TSV.

The difference in the bending beam behaviors could be due to the different plasticity effects. For $\Delta T = 200\,^{o}\mathrm{C}$, the von-Mises stresses in the Cu for the three structures were calculated by elastic FEA models, as shown in Fig. 3.18a-b. In the Cu thin film and the annular TSV, the stresses are nearly uniform and plastic deformation occurs over the entire volume of Cu, as shown in Fig. 3.16a-b. In contrast, the stress is non-uniform in the fully-filled Cu vias (Fig. 3.14c), and the von-Mises stress reaches the yield strength only in a small region near the junction between the via/Si interface and the upper surface. As a result, the plastic deformation in the fully-filled Cu vias is highly localized. Therefore, the bending beam measurements, with or without the hysteresis, provide qualitative evaluations of the plasticity effects in different structures.



(a) (b)

Figure 3.18: Comparison of von-Mises stresses between the thin film and TSVs structures: (a) Thin film; (b) Annular TSV.

3.2 RAMAN SPECTROSCOPY

3.2.1 Background of Raman theory

Among several potential techniques for local stress measurement, micro-Raman spectroscopy appears particularly promising and was recently applied to measure the local stress distribution in Si near Cu TSVs [61, 98, 99]. This method is a spectroscopic technique where the stress magnitude is deduced from the frequency shift of the impinging laser light as a result of inelastic scattering by Si lattice [100-102]. The lateral resolution of micro Raman spectroscopy is in the order of 0.5 μm, depending on the laser wavelength and the substrate lattice [102]. For Si, the Raman penetration depth ranges up to ~ 2 μm, again depending on the laser wavelength. Moreover, this technique can be used to measure the near-surface stresses in Si around TSVs even with an oxide layer covering the wafer surface because the laser can penetrate the oxide layer with nearly 95% transparency.

In this section, the fundamental theory of Raman spectroscopy is reviewed briefly. The effect of strain (ε_{ij}) on the Raman modes in (001) silicon is described by the secular equation [100],

$$\begin{vmatrix} p\varepsilon_{11}+q(\varepsilon_{22}+\varepsilon_{33}) & 2r\varepsilon_{12} & 2r\varepsilon_{13} \\ 2r\varepsilon_{12} & p\varepsilon_{22}+q(\varepsilon_{33}+\varepsilon_{11}) & 2r\varepsilon_{23} \\ 2r\varepsilon_{13} & 2r\varepsilon_{23} & p\varepsilon_{33}+q(\varepsilon_{11}+\varepsilon_{22}) \end{vmatrix} - \lambda \mathrm{I} = 0 , \qquad (3.3)$$

where p, q, r are material parameters representing the phonon deformation potential, with $p=-1.43\omega_0^2$, $q=-1.89\omega_0^2$, and $r=-0.59\omega_0^2$ [101], and $\omega_o \sim 520.8\,\mathrm{cm}^{-1}$ is the Raman frequency of the unstrained crystal. The eigenvalues (λ_i) of the secular equation give the Raman frequency shift.

$$\Delta\omega_i = \omega_i - \omega_0 \approx \frac{\lambda_i}{2\omega_0} \ (i=1\sim 3) . \qquad (3.4)$$

Assuming linear elasticity, the strain components are related to the stress components (σ_{ij}) by Hooke's law:

$$\begin{Bmatrix} \varepsilon_{11} \\ \varepsilon_{22} \\ \varepsilon_{33} \\ 2\varepsilon_{23} \\ 2\varepsilon_{13} \\ 2\varepsilon_{12} \end{Bmatrix} = \begin{bmatrix} S_{11} & S_{12} & S_{12} & 0 & 0 & 0 \\ S_{12} & S_{11} & S_{12} & 0 & 0 & 0 \\ S_{12} & S_{12} & S_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & S_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & S_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & S_{44} \end{bmatrix} \begin{Bmatrix} \sigma_{11} \\ \sigma_{22} \\ \sigma_{33} \\ \sigma_{23} \\ \sigma_{13} \\ \sigma_{12} \end{Bmatrix}, \tag{3.5}$$

where $S_{11} = 7.68\times10^{-12}$ Pa^{-1}, $S_{12} = -2.14\times10^{-12}$ Pa^{-1}, and $S_{44} = 12.7\times10^{-12}$ Pa^{-1} are the elastic compliance of Si.

The second rank Raman tensors describing three optical modes for the unstrained Si crystal are

$$R_1 = \begin{pmatrix} 0 & 0 & 0 \\ 0 & 0 & d \\ 0 & d & 0 \end{pmatrix}, \; R_2 = \begin{pmatrix} 0 & 0 & d \\ 0 & 0 & 0 \\ d & 0 & 0 \end{pmatrix}, \; R_3 = \begin{pmatrix} 0 & d & 0 \\ d & 0 & 0 \\ 0 & 0 & 0 \end{pmatrix}. \tag{3.6}$$

Under the effect of strain, the Raman tensors become [103-105],

$$R'_i = \sum_{k=1}^{3} R_k \left(v'_i \cdot v_k \right), \tag{3.7}$$

where v'_i and v_k are the eigenvectors of the secular equation with and without the strain, respectively.

The intensity of the Raman signal for each optical mode is

$$I_k = C \left| e_i \cdot R'_k \cdot e_s \right|^2, \tag{3.8}$$

where e_i and e_s represent the polarization vectors of the incident and scattered light, respectively, and C is a scalar constant. Most Raman systems have a backscattering configuration, where the incident light is nearly perpendicular to the sample surface. For backscattering from (001) Si surface, both the incident and scattering vectors, e_i and e_s, can be assumed parallel to the surface plane. The relationship between the Raman

intensity and the polarization vectors in Eq. (3.8) suggests the possibility to select a specific Raman mode by properly choosing the polarization of the incident and scattered light. In the case of unstrained silicon, there are three degenerate optical modes, having the same frequency ($\omega_o \sim 520\,\mathrm{cm}^{-1}$) but different polarizations [105]: two transverse optical modes (TO) and one longitudinal optical (LO) mode. However, with strain, the three optical modes in general have different frequencies (ω_i) and different intensities (I_i), corresponding to three Raman peaks. When the three Raman peaks are indistinguishably close, the average frequency shift is taken as [103],

$$\Delta\omega = \frac{I_1\Delta\omega_1 + I_2\Delta\omega_2 + I_3\Delta\omega_3}{I_1 + I_2 + I_3} \quad . \tag{3.9}$$

Now consider a specific example. On the (001) Si surface, the stress is assumed to be biaxial along the [110] direction, represented as (σ_r, σ_θ) in a cylindrical coordinate. In the reference coordinate with respect to the crystal axes, the stress components are

$$\sigma_{11} = \sigma_{22} = \frac{\sigma_r + \sigma_\theta}{2}, \tag{3.10}$$

$$\sigma_{12} = \frac{\sigma_r - \sigma_\theta}{2}, \tag{3.11}$$

$$\sigma_{31} = \sigma_{32} = \sigma_{33} = 0. \tag{3.12}$$

By Eq. (3.5), the strain components are obtained as

$$\varepsilon_{11} = \varepsilon_{22} = \frac{S_{11} + S_{12}}{2}\left(\sigma_r + \sigma_\theta\right), \tag{3.13}$$

$$\varepsilon_{33} = S_{12}(\sigma_{11} + \sigma_{22}) = S_{12}(\sigma_r + \sigma_\theta), \tag{3.14}$$

$$\varepsilon_{12} = \frac{S_{44}}{2}\sigma_{12} = \frac{S_{44}}{4}(\sigma_r - \sigma_\theta), \tag{4.15}$$

$$\varepsilon_{13} = \varepsilon_{23} = 0. \tag{3.16}$$

Insert Eqs. (3.13~16) into the secular equation (3.3), and the eigenvalues are obtained as

$$\begin{aligned}\lambda_1 &= \frac{p(\varepsilon_{11}+\varepsilon_{22})+q(\varepsilon_{11}+\varepsilon_{22}+2\varepsilon_{33})+4r\varepsilon_{12}}{2} \\ &= \frac{p(S_{11}+S_{12})+q(S_{11}+3S_{12})}{2}(\sigma_r+\sigma_\theta)+\frac{rS_{44}}{2}(\sigma_r-\sigma_\theta)\end{aligned}, \tag{3.17}$$

$$\begin{aligned}\lambda_2 &= \frac{p(\varepsilon_{11}+\varepsilon_{22})+q(\varepsilon_{11}+\varepsilon_{22}+2\varepsilon_{33})-4r\varepsilon_{12}}{2} \\ &= \frac{p(S_{11}+S_{12})+q(S_{11}+3S_{12})}{2}(\sigma_r+\sigma_\theta)-\frac{rS_{44}}{2}(\sigma_r-\sigma_\theta)\end{aligned}, \tag{3.18}$$

$$\begin{aligned}\lambda_3 &= p\varepsilon_{33}+q(\varepsilon_{11}+\varepsilon_{22}) \\ &= \left[pS_{12}+q(S_{11}+S_{12})\right](\sigma_r+\sigma_\theta)\end{aligned}. \tag{3.19}$$

In a backscattering configuration with $e_i=(110)$ and $e_s=(100)$, the Raman intensities are zero for the first two modes ($I_1=I_2=0$), and only the third Raman mode is detectable ($I_3\neq 0$). Thus, by Eq. (3.4), the Raman shift for the third mode is related to the stress components as

$$\Delta\omega_3 \approx \frac{\lambda_3}{2\omega_0}=\frac{pS_{12}+q(S_{11}+S_{12})}{2\omega_0}(\sigma_r+\sigma_\theta). \tag{3.20}$$

To determine the effective proportionality factor between the Raman shift and the stress sum for the specific experimental conditions, calibration measurements by high-resolution XRD on an equi-biaxially stressed film system were conducted, yielding the relation [98].

$$\sigma_r+\sigma_\theta\ (\text{MPa})=-470\Delta\omega_3(\text{cm}^{-1}). \tag{3.21}$$

The obtained sensitivity factor corresponds to phonon deformation potential parameters in between of the values derived by Chandrasekhar [106] and Anastassakis [107]. Note that the reference frequency ω_o also depends on the system calibration, typically with $\pm 0.02\,\text{cm}^{-1}$ spectral resolution, which corresponds to a stress resolution of ~10 MPa [108,

109]. In the present investigation, this quantity was determined at positions far away from the TSVs assuming that the stress level there was below the minimum detection level.

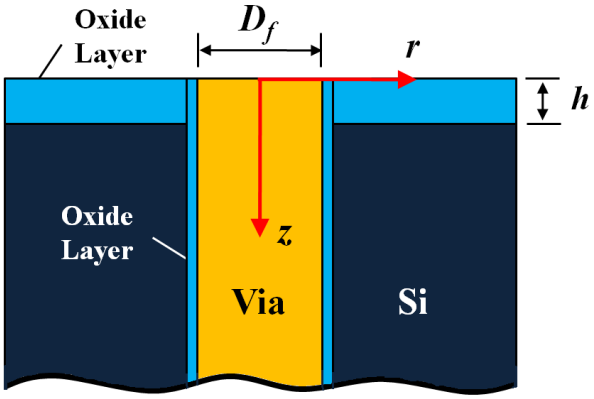
3.2.2 Experimental description[2]

The TSV specimen consists of a periodic array of Cu vias of diameter $D_f = 10\,\mu m$ with pitch distances of 40 μm in $[110]$ direction and 50 μm in $[1\bar{1}0]$ direction, respectively. The TSV structure near the wafer surface is schematically shown in Figure 3.19a. An oxide layer of about 0.4 μm thickness and a thin Ta barrier layer were deposited at the side wall between the via and Si. The surface of the Si wafer was covered by an oxide layer of about 0.8 μm thickness; for some measurements the surface oxide layer were mechanically polished off. The wafer thickness was 700 μm, and the TSV depth was around 55 μm.

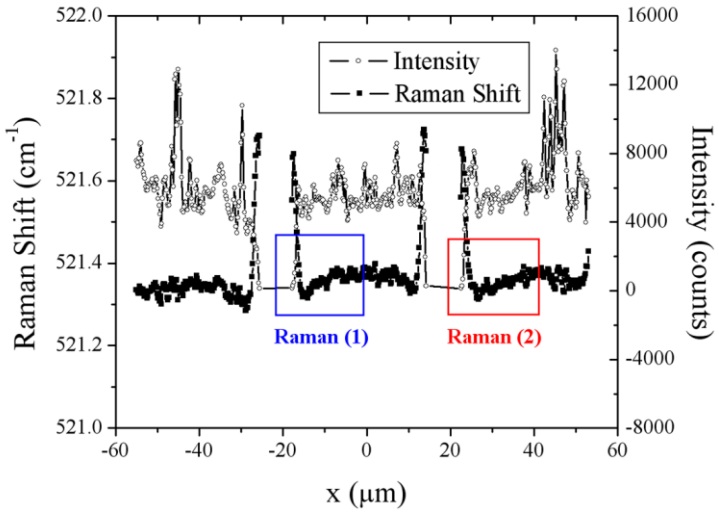
A Jobin Yvon spectrometer HR800 was used for the Raman measurements, equipped with 442 nm Ar excitation laser and a focused spot size of about 0.8 μm by a 100x objective (NA = 0.9). The penetration depth (d) of the laser radiation is approximately 250 nm into Si in this case. Figure 3.19b shows the measured Raman intensity and frequency around two neighboring vias obtained by a line scan in the [110] direction. The drop in the intensity of the Raman signal indicates the locations of the Si/TSV interface. Close to the Si/TSV interface, the Raman frequency first drops and then rises abruptly. With Eq. (3.22) and a calibrated reference frequency, ω_o, the sum of the two principal stresses in Si can be deduced directly from the Raman frequency shift, which presumably is a volume average over the region defined by the area of the focused spot and the penetration depth of the laser. As shown in Chapter 2, the near-surface stress

[2] *In collaboration with Qiu Zhao, The University of Texas at Austin and Michael Hecker, GLOBALFOUNDRIES*

field induced by differential thermal expansion around a TSV is non-uniform in both in-plane and depth directions. Therefore, it is important to interpret the micro-Raman measurement along with a detailed stress analysis.



(a)



(b)

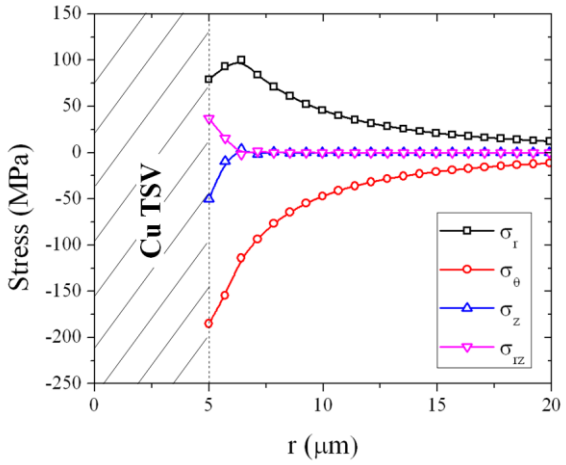
Figure 3.19: (a) Schematic of a fully filled TSV structure near the wafer surface; (b) Measured Raman intensity (unfilled symbols) and frequency (filled symbols) around two copper TSVs in a periodic array.

3.2.3 Analysis of near-surface stresses

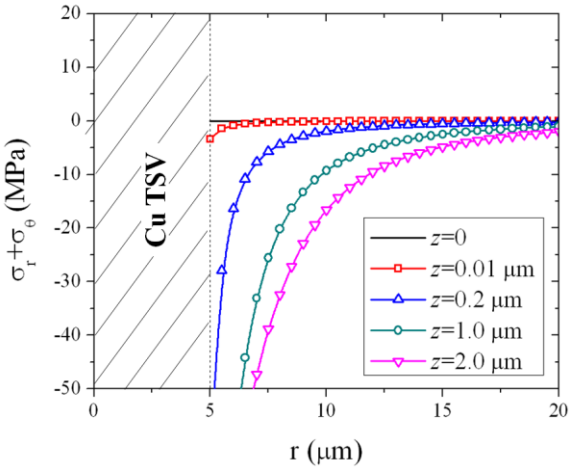
The stress field induced by differential thermal expansion around a circular TSV embedded in a Si wafer was obtained approximately by the method of superposition in Chapter 2. Using the 3-D analytic solution, the sum of in-plane stresses is studied in comparison with the Raman measurements. With Eqs. (2.1), (2.6) and (2.7), the sum of the radial and circumferential stresses in the TSV structure is obtained as

$$\sigma_r(r,z)+\sigma_\theta(r,z)=\frac{-E\varepsilon_T}{2\pi(1-\nu)}\int_0^{\frac{D_f}{2}}\int_0^{2\pi}\left(\frac{3z^3}{R^5}-\frac{2(1+\nu)z}{R^3}\right)\rho\, d\rho\, d\theta\,. \tag{3.22}$$

By Eq. (3.22), it is found that the stress sum is identically zero both at the wafer surface ($z=0$) and far away from the surface ($z\to\infty$). In between, the stress sum varies with the depth (z) in the near-surface region as shown in Fig. 3.20b. The stress sum is negative everywhere for $z>0$ and $r>D_f/2$, whereas the magnitude decays monotonically as *r* increases and diminishes far away from the via. Since the two stress components have opposite signs as shown in Fig. 3.20a, the magnitude of their sum is relatively small. Near the wafer surface ($z<2$ μm), the magnitude of the stress sum increases with increasing depth. This suggests that the Raman signal depends on the laser penetration depth and an optimal penetration depth may be determined for the Raman measurement. On the other hand, while the stress magnitude is increasingly high approaching the Si/TSV interface, the Raman signal as shown in Fig. 3.19b becomes noisy due to the reduction in the Raman intensity. Thus, the Raman data very close to the interface shall be interpreted with caution.



(a)



(b)

Figure 3.20: Near-surface stresses around an isolated TSV predicted by the semi-analytical solution ($\Delta T = -100\,^{\circ}\mathrm{C}$, $D_f = 10\,\mu\mathrm{m}$). (a) Stress components at $z = 0.2\,\mu\mathrm{m}$; (b) Sum of the in-plane normal stresses at different depths.

Next, we lift the two major assumptions made in the semi-analytical solution by numerical analyses based on the finite element method. First, the heterogeneous materials in the TSV structure are considered with different elastic moduli for the via material and the oxide layer, both taken to be linear elastic and isotropic, with $E_f = 110\,\mathrm{GPa}$ and $\nu_f = 0.35$ for the Cu TSV, and $E_o = 70\,\mathrm{GPa}$ and $\nu_o = 0.16$ for the oxide layer. The thin

Ta layer has negligible effect on the stress state in Si, thus ignored in the finite element analysis (FEA). Second, the elastic anisotropy of Si is taken into account by using the anisotropic elastic constants for Si crystal with a cubic symmetry as in Eq. (3.5).[110] As shown in Fig. 3.21a, the 3-D FEA model consists of three different materials (Cu, Oxide, and Si), without the surface oxide layer. The effect of surface oxide layer is discussed in the next section. To simulate the periodic TSV array used for the Raman measurements, symmetric boundary conditions are applied to the side faces in $[110]$ and $[1\bar{1}0]$ directions with different pitch distances (40 μm and 50 μm, respectively). Furthermore, by symmetry, only a quarter of the via is modeled. To further reduce the computational model, the wafer thickness is taken to be 100 μm in the FEA model instead of 700 μm in the real specimen, while the TSV depth is 55 μm. The top surface is traction free, and the out-of-plane displacement (*z*-direction) at the bottom surface is set to be zero. With such a boundary condition, increasing the wafer thickness has negligible effect on the near-surface stress distribution. Linear 3-D solid elements (C3D8R) in ABAQUS are used, with a fine mesh near the surface (element size = 0.1 μm in the thickness direction and 0.2 μm in the lateral direction) and an increasingly coarse mesh away from the surface and TSV.

The contours of the stress sum, $\sigma_r + \sigma_\theta$, calculated at the depth $z = 0.2\,\mu\text{m}$ is shown in Fig. 3.21b-c. For comparison, Fig. 3.21b shows the result from an isotropic Si model with $E_m = 130\,\text{GPa}$ and $\nu_m = 0.28$, where the stress field is axi-symmetric with concentric circular contours for the stress sum. Unlike the results for an isolated TSV shown in Fig. 3.20b, the stress sum in Si becomes positive except for the regions very close to the via, due to the interaction between neighboring vias in the periodic array. Using the anisotropic elastic property for the (001) Si, the stress distribution as shown in

Fig. 3.21c exhibits a four-fold symmetry, reflecting the cubic symmetry of the Si crystal. Due to the different pitch distances in the $[110]$ and $[1\bar{1}0]$ directions, the stress variation is slightly different in the two directions. This result suggests that, due to the elastic anisotropy of Si and the via-via interactions, the near-surface stress measured by Raman spectroscopy could depend on the direction of Raman scanning. To quantitatively examine the directional dependence of Raman signal for the (001) Si wafer, we show in Fig. 3.22 the stress sum along different directions of line scanning, by varying the angle θ from the $[110]$ direction. In particular, we note that, along the $[110]$ direction ($\theta = 0^{\circ}$), the magnitude of the stress sum reaches a positive peak at $r \sim 10\,\mu\text{m}$. The magnitude of the positive peak stress is around 30 MPa. A previous study has reported qualitatively similar variation of the stress by Raman measurements but with a higher positive peak stress (~50 MPa).[99] Among all the directions shown in Fig. 3.22, relatively strong Raman signal is expected along the $[110]$ direction. However, the difference among all angles is less than 20 MPa, close to the stress resolution for the Raman measurement. Thus it may be practically difficult to measure the directional dependency using the Raman spectroscopy.

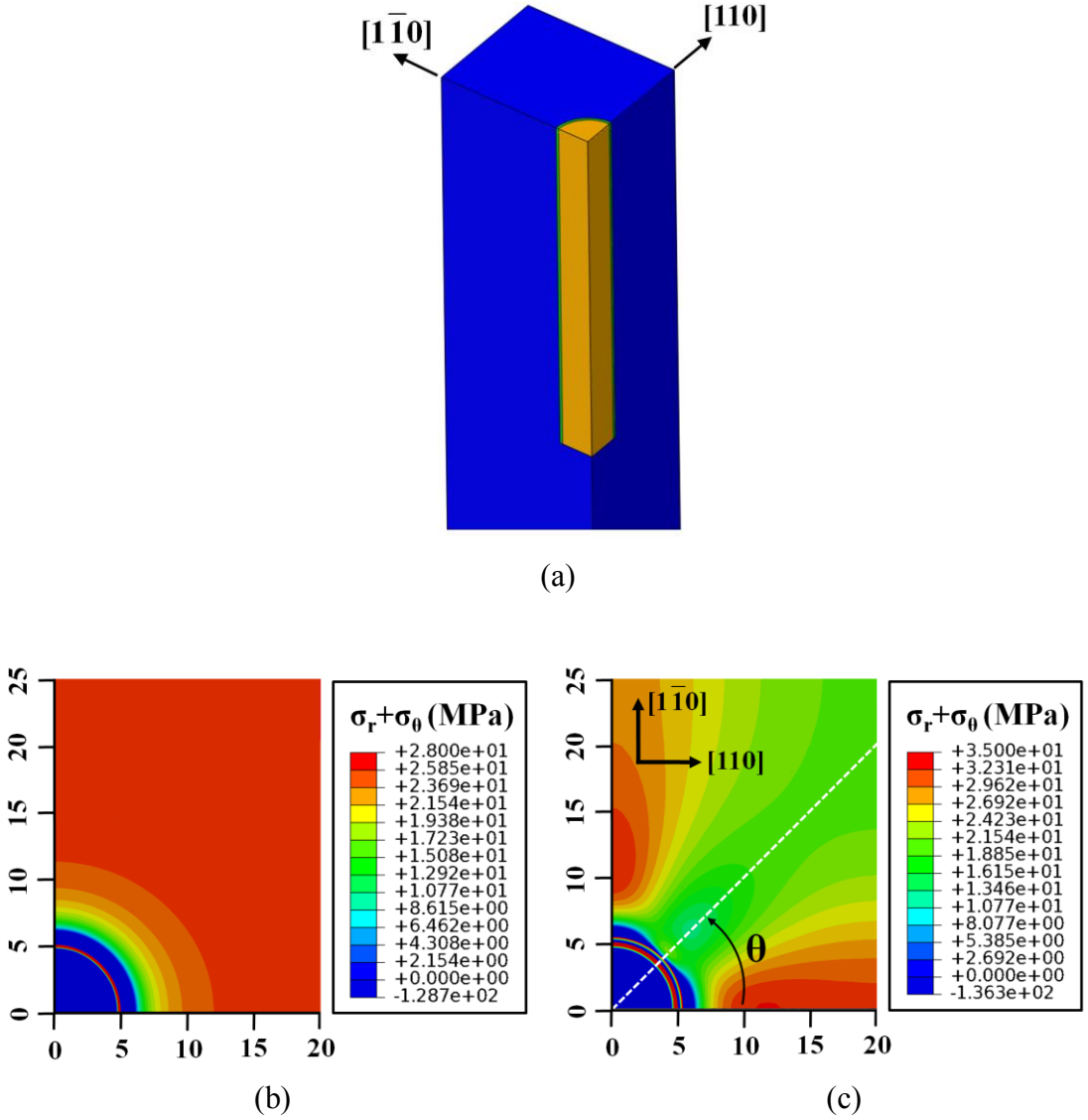


Figure 3.21: (a) Part of the 3D FEA model showing a quarter of the Cu via (orange) embedded in Si (blue) along with a thin oxide layer (green) at the interface. (b) and (c) show distributions of the stress sum ($\sigma_r + \sigma_\theta$) near the wafer surface ($z = 0.2\,\mu\text{m}$) for an isotropic Si model and an anisotropic (001) Si wafer, respectively.

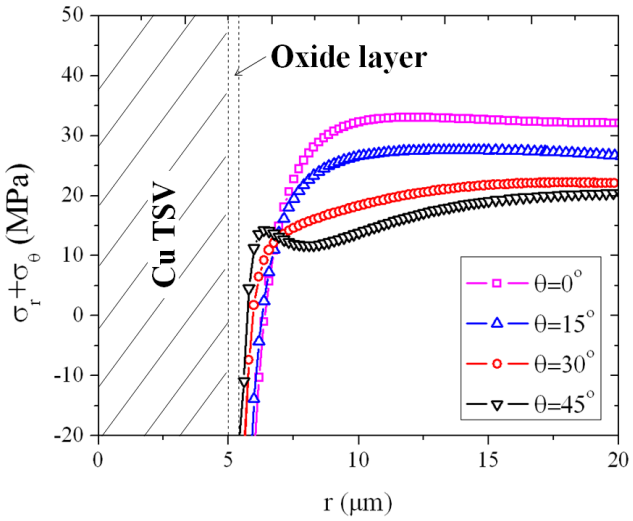


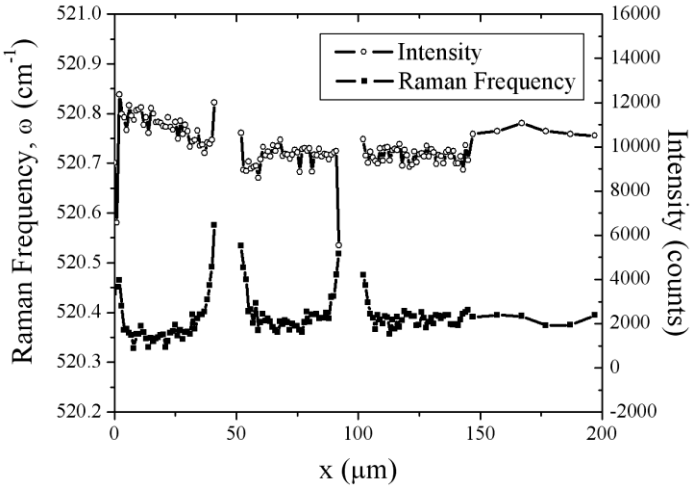
Figure 3.22: Directional dependence of the stress distribution for (001) Si wafer ($\Delta T = -100$ ºC, $D_f = 10\,\mu$m, and $z = 0.2\,\mu$m).

3.2.4 Comparison between Raman and FEA results

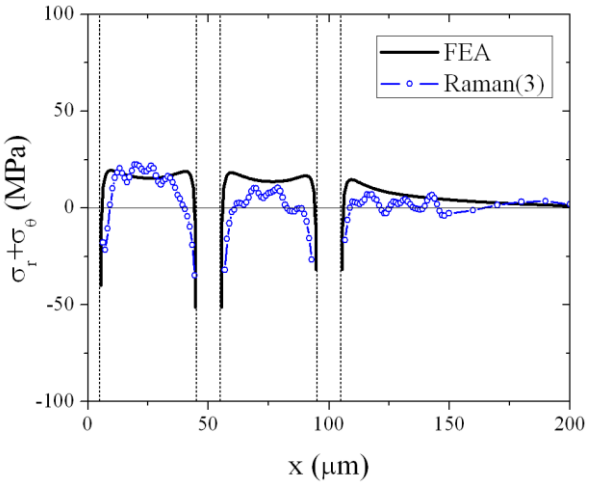
Using Eq. (3.21), the measured Raman frequencies can be converted to the stress sum. To determine the reference frequency, ω_o, the Raman scans were not only performed between the vias but also extended to the bare silicon surface far away from the vias where the stress sum is expected to be zero. As shown in Fig. 3.23a, the average Raman frequency obtained from the far-field measurement gives the reference frequency, $\omega_o = 520.39\,\text{cm}^{-1}$. For this measurement, the surface oxide layer on the TSV sample was mechanically polished, and the sample was subsequently subject to an anneal step at 200°C. All the Raman measurements were done after cooling down to the room temperature.

The Raman data in Fig. 3.23a is similar to those in Fig. 3.19b for the specimen with the surface oxide layer, but the frequency is slightly lower for the specimen without the surface layer. The effect of surface oxide layer is discussed further in the next section.

In Fig. 3.23b, we convert the measured Raman frequencies to stresses by Eq. (3.22) using $\omega_o = 520.39\,\text{cm}^{-1}$, in comparison with the stresses obtained from the FEA model. For the FEA model, the materials are assumed to be linear elastic as described in section 3.2.3. As a result, the stress magnitude from the FEA model depends linearly on the temperature change, ΔT, from a reference temperature at which the stress is zero. Based on the bending beam measurements (Fig. 3.6), the reference temperature for the TSV specimen was determined to be around 100°C, and thus $\Delta T = -70\,°\text{C}$ for the Raman measurements at the room temperature (~30°C). With $\Delta T = -70\,°\text{C}$ the results from the FEA model are in reasonable agreement with the Raman data as shown in Fig. 3.23b. We note that the stress magnitude is relatively low in this case, which makes it difficult for the Raman measurement due to the relatively large noise-to-signal ratio.



(a)

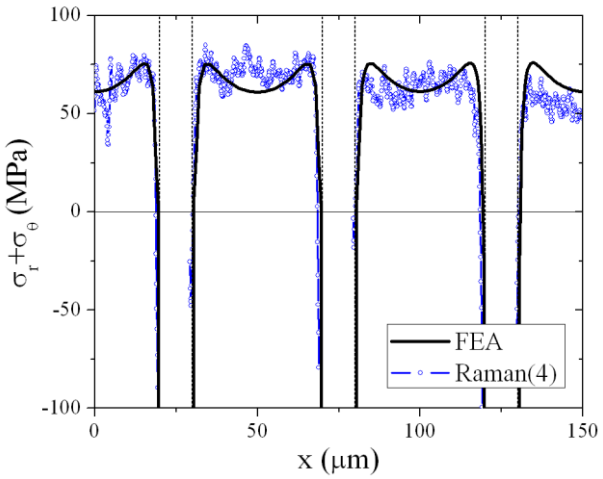


(b)

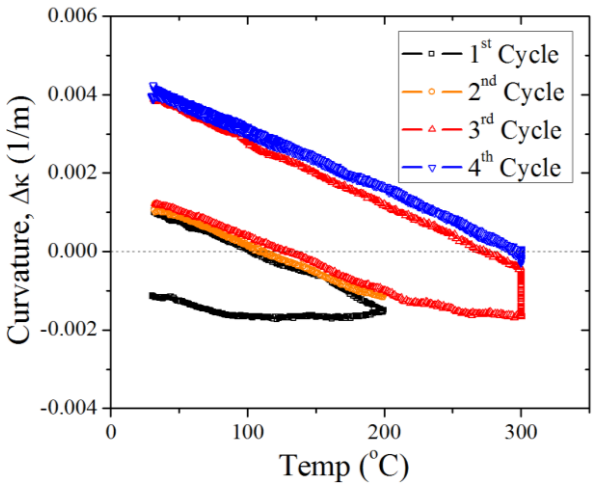
Figure 3.23: (a) Measured Raman intensity and frequency for a TSV specimen with the surface oxide layer polished off. (b) Comparison of the near-surface stress distribution between Raman measurements and finite element analysis (FEA). Vertical dash lines indicate the Cu/Si interfaces.

Additional Raman measurements were performed for the TSV samples annealed at 300°C for 1 hr. In Fig. 3.24, the stresses from the Raman measurements were compared to the FEA result with $\Delta T = -270\,^{\circ}\mathrm{C}$. For the stress conversion, the same

reference frequency ($\omega_o = 520.39\,\text{cm}^{-1}$) was used. It was observed that annealing at 300°C relaxed most of the stresses in the TSV specimen, as shown by the bending beam measurements in Fig. 3. 24b. Thus, the reference temperature for the induced thermal stresses was raised to 300°C. Upon cooling down to the room temperature, the stress magnitude in Si has increased due to the higher reference temperature [62].



(a)



(b)

Figure 3.24: (a) Comparison of the near-surface stress distribution between Raman measurements and finite element analysis (FEA), for a TSV specimen annealed at 300°C for 1hr. (b) BB test result for a TSV specimen annealed at 300°C for 1hr.

3.2.5 Effect of surface oxide layer

With an oxide layer on the wafer surface as illustrated in Fig. 3.19a, the measured Raman frequencies in Fig. 3.19b were converted to stresses by Eq. (3.22), as shown in Fig. 3.25. Here, a different reference frequency was used ($\omega_o = 521.44\,\text{cm}^{-1}$) since this measurement was performed using a different Raman system. The presence of the oxide layer is not expected to change the reference frequency. Assuming similar penetration depth (~0.2 μm) in the Si, the stress state measured by Raman is at z = 1.0 μm, which is slightly different from the case without the surface oxide layer (h = 0.8 μm). As shown in Fig. 3.23, with the surface oxide layer, the tensile stress is lower and the compressive stress is higher in Si, according to the FEA model ($\Delta T = -100\,^{o}\text{C}$).

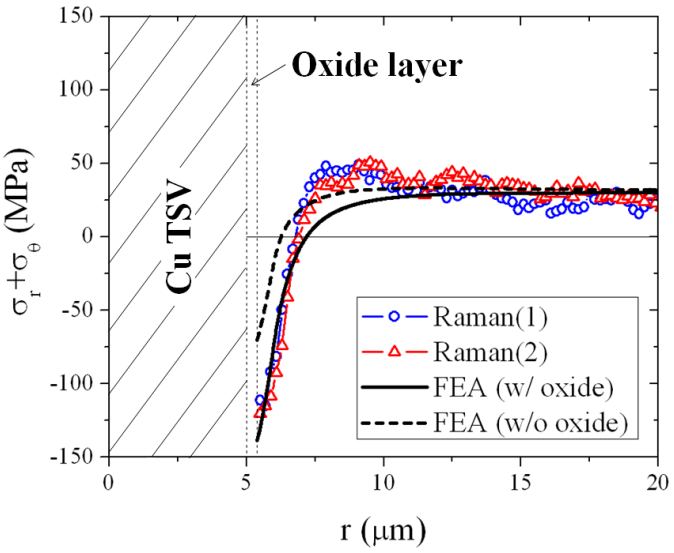


Figure 3.25: Comparison of the near-surface stress distribution between Raman measurements and finite element analysis (FEA) around a Cu TSV in (001) Si wafer with a surface oxide layer. Vertical dash lines indicate the Cu/barrier and barrier/Si interfaces.

The FEA results compare closely with the Raman results except for a region with 7 μm < r < 10 μm, where the Raman measurements have a peak tensile stress of around 50 MPa. Similar peak stresses were observed in the previous studies [111]. The FEA model without the surface oxide layer does predict a peak tensile stress of similar magnitude (see Fig. 3.24). With the surface oxide layer, however, no peak stress is observed from the FEA model.

3.2.6 Effect of plasticity

The thermal stresses in the Cu vias may cause plastic deformation, which in turn may influence the stresses in Si. In Chapter 2, the effect of plasticity on stresses in TSV structures has been discussed. It is found that plastic deformation is largely confined in a relatively small region near the junction between the Cu/via interface and the surface (Fig. 2.9). As a result, the stress in Si around the via changes slightly near the interface but not much elsewhere. Figure 3.26 plots the stress sum in Si at r = 20 μm as a function of the temperature change, comparing the results from the all-elastic model and three elastic-plastic models with different yield strengths, σ_y. The stress in Si increases linearly with the temperature change in the all-elastic model. With plastic deformation in the via, the stress deviates from the linear behavior, depending on the yield strength. In addition to the plastic deformation, grain growth in the metal vias has been observed during thermal cycling,[62] which could relax the thermal stress in the vias and thus further reduce the stress in Si.

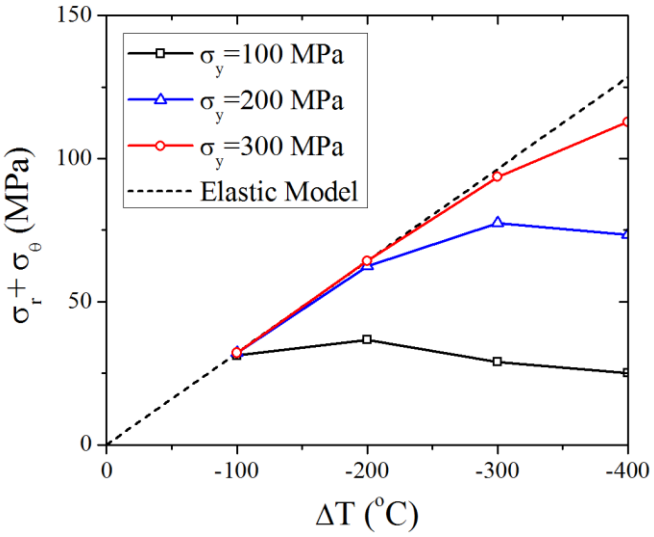


Figure 3.26: Effect of Cu plasticity on the stress in Si.

3.3 SUMMARY

Two experimental methods have been employed to study the thermomechanical behaviors of TSV structures. The bending beam technique measures stress-induced deformation of the TSV specimens during thermal cycling. Combined with finite element analysis, the thermal stresses in the TSV structures can be evaluated. The observed inelastic behavior is attributed to microstructural evolution of the Cu vias, while the localized plastic deformation may be responsible for via extrusion.

Using the Raman spectroscopy, the local distribution of near-surface stress in Si has been measured, in comparison with stress analysis of the TSV structure based on a semi-analytic approach and finite element analysis. In particular, the depth dependence of the stress distribution and the effect of elastic anisotropy of Si have to be considered for interpreting the Raman data. The effects of the surface oxide layer and plasticity on the Raman measurements are discussed.

Together, the two experimental methods provide a complementary approach for characterizing thermomechanical behaviors of the TSV structures.

Chapter 4

Interfacial Reliability for TSV Structures

The stress analysis performed in Chapter 2 suggested a potential failure mechanism of the TSV structure due to interfacial delamination. In this chapter, focus is directed on the analysis of interfacial reliability for TSV structures. Figure 4.1 depicts two modes of interfacial delamination for a fully-filled TSV structure. With a negative thermal load ($\Delta T < 0$), the radial stress along the via/Si interface is tensile (assuming $\alpha_f > \alpha_m$). Consequently, the interfacial delamination crack may grow in a mixed mode (peeling and shearing) [112-114]. With a positive thermal load ($\Delta T > 0$), however, the radial stress is compressive which does not contribute to the driving force for delamination. This results in an interfacial crack with a pure shearing mode (mode II). In this case (Fig. 4.1b), the two crack faces are in contact and may be subjected to friction. For simplicity, however, a frictionless contact [115] is assumed in the present study. First, analytical solutions are developed for the steady-state energy release rate of the interfacial crack, under both cooling and heating conditions. The analytical solutions are then compared to the numerical results by finite element analysis, to study the effects of crack length and wafer thickness on the fracture driving force. Based on these results, the effects of the TSV materials and geometries on interfacial reliability will be discussed in Chapter 5 from material selection and structural design considerations. Furthermore, an analytical cohesive zone model is developed in this Chapter to investigate initiation of interfacial delamination. For verification of the analytic model, finite element simulations are performed with cohesive elements for the interface.

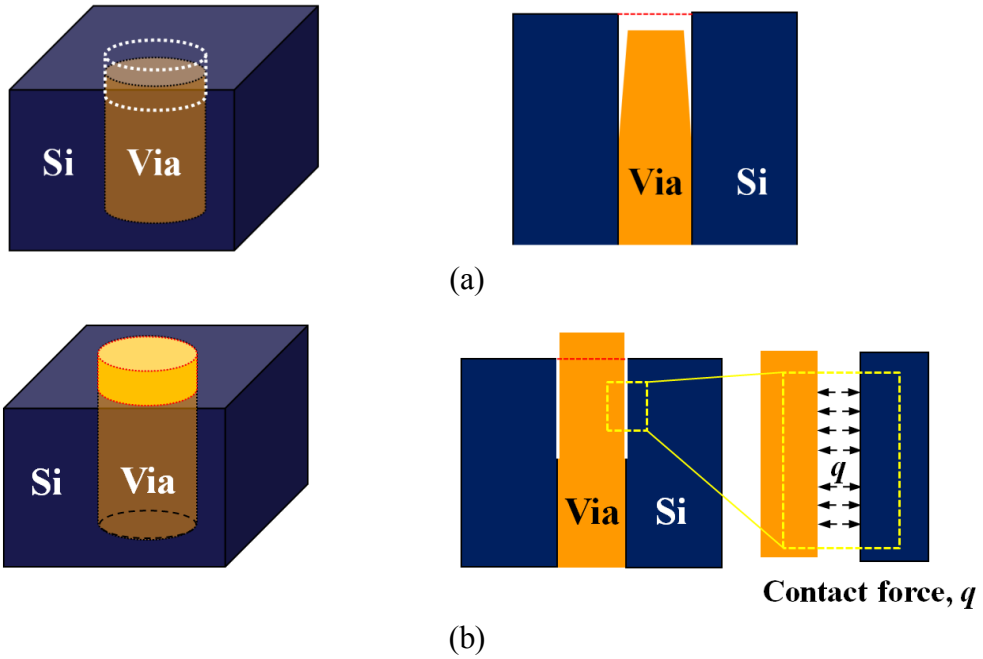


Figure 4.1: Schematics of interfacial delamination of TSV under cooling and heating conditions. In both cases, the interfacial crack is assumed to grow axi-symmetrically from the top surface: (a) Cooling ($\Delta T < 0$): Mode I+II; (b) Heating ($\Delta T > 0$): Mode II.

4.1 STEADY-STATE DELAMINATION

For a TSV with a relatively high aspect ratio (H / D_f), the energy release rate for interfacial delamination reaches a steady state when the crack length is several times greater than the via diameter [116]. Since the energy release rate is usually lower for shorter cracks, the steady-state value sets an upper bound for the fracture driving force, which may be used as a conservative design parameter for reliable TSV structures.

Consider an infinitely long fiber (TSV) in an infinite matrix (Si wafer), with a semi-infinite, circumferential crack along the interface and subjected to a thermal load (ΔT).While the stress field near the crack front is complicated with singularity and 3D distribution, it translates invariably as the crack front advances in a steady state. Thus, the

steady-state energy release rate for the interfacial crack growth (per unit area) can be obtained by comparing the elastic strain energy far ahead of the crack front and that far behind the crack front. Far ahead of the crack front, the stress field can be obtained analytically by solving the 2D plane-strain problem (Problem A in Fig. 2.2b). Far behind the crack front, since the TSV is debonded from Si, the stress is relaxed in both the via and Si. For the case of cooling ($\Delta T < 0$), the stress is zero in both TSV and Si. For heating ($\Delta T > 0$), however, the contact between the crack faces induces a stress field similar to Problem A, but the axial stress (σ_z) in the via is zero under the assumption of frictionless contact. Based on Eqs. (2.1-3), the elastic strain energy densities (per unit volume) in the TSV and Si far ahead of the crack front are, respectively,

$$U_f^A = \frac{1}{2} E_f \varepsilon_T^2 \left[1 + \frac{2(1-2\nu_f)(1+\nu_f)}{\left(1-2\nu_f + \frac{1+\nu_m}{1+\nu_f}\frac{E_f}{E_m} \right)^2} \right], \tag{4.1}$$

$$U_m^A = E_f \varepsilon_T^2 \frac{(1+\nu_m) E_f / E_m}{\left(1-2\nu_f + \frac{1+\nu_m}{1+\nu_f}\frac{E_f}{E_m} \right)^2} \left(\frac{D_f}{2r} \right)^4 . \tag{4.2}$$

For the case of cooling, the release of the elastic energy per unit length of the interfacial crack is,

$$\Delta U_{cooling} = \frac{\pi}{4} D_f^2 U_f^A + 2\pi \int_{D_f/2}^{\infty} U_m^A(r) r dr . \tag{4.3}$$

The steady-state energy release rate (per unit area) is thus

$$G_{cooling}^{SS} = \frac{\Delta U_{cooling}}{\pi D_f}$$
$$= \frac{E_m \varepsilon_T^2 D_f}{4}\left(\frac{(1+\nu_f)(1+\alpha)}{(1-2\nu_f)(1-\alpha)+(1+\alpha)\dfrac{1+\nu_m}{1+\nu_f}} + \frac{1}{2}\frac{1+\alpha}{1-\alpha} \right), \tag{4.4}$$

where $\alpha = \left(\bar{E}_f - \bar{E}_m\right)/\left(\bar{E}_f + \bar{E}_m\right)$ is the Dundurs' parameter for elastic mismatch between the TSV and Si, with $\bar{E} = E/\left(1-\nu^2\right)$. If the elastic mismatch is neglected (i.e., $\alpha = 0$ and $\nu_f = \nu_m = \nu$), Eq. (4.4) is reduced to a simpler form:

$$G_{cooling}^{SS} = \frac{E\varepsilon_T^2 D_f}{4(1-\nu)}. \tag{4.5}$$

Under the heating condition ($\Delta T > 0$), due to the contact of the crack faces (Fig. 4.1b), the stress state in the TSV far behind the crack front is equi-biaxial:

$$\sigma_r = \sigma_\theta = -\frac{E_f \varepsilon_T}{1-\nu_f+(1+\nu_m)\dfrac{E_f}{E_m}}. \tag{4.6}$$

Correspondingly, the stress field in the matrix (Si) is

$$\sigma_r = -\sigma_\theta = -\frac{E_f \varepsilon_T}{1-\nu_f+(1+\nu_m)\dfrac{E_f}{E_m}}\frac{D_f^2}{4r^2}. \tag{4.7}$$

The elastic strain energy densities (per unit volume) of the TSV and Si far behind the crack front are, respectively,

$$U_f^C = \frac{E_f \varepsilon_T^2 (1-\nu_f)}{\left[1-\nu_f+(1+\nu_m)\dfrac{E_f}{E_m}\right]^2}, \tag{4.8}$$

$$U_m^C = E_f \varepsilon_T^2 \frac{(1+\nu_m)E_f / E_m}{\left[1-\nu_f+(1+\nu_m)\frac{E_f}{E_m}\right]^2}\left(\frac{D_f}{2r}\right)^4. \tag{4.9}$$

Therefore, the release of the elastic strain energy per unit length of the interfacial crack is

$$\Delta U_{heating} = \frac{\pi}{4} D_f^2 \left(U_f^A - U_f^C\right) + 2\pi \int_{D_f/2}^{\infty} \left(U_m^A - U_m^C\right) r dr \,. \tag{4.10}$$

The steady-state energy release rate for heating is then

$$G_{heating}^{SS} = \frac{\Delta U_{heating}}{\pi D_f}$$

$$= \frac{E_m \varepsilon_T^2 D_f}{4}\left[\frac{(1+\alpha)(1+\nu_f)}{(1-\alpha)(1-2\nu_f)+(1+\alpha)\frac{1+\nu_m}{1+\nu_f}} + \frac{1}{2}\frac{1+\alpha}{1-\alpha} - \frac{(1+\alpha)}{(1-\nu_f)(1-\alpha)+(1+\nu_m)(1+\alpha)}\right]. \tag{4.11}$$

Again, a simpler result can be obtained by neglecting the elastic mismatch, namely

$$G_{heating}^{SS} = \frac{1+\nu}{8(1-\nu)} E \varepsilon_T^2 D_f \,. \tag{4.12}$$

Several interesting results can be deduced based on the analytical solutions for the steady-state energy release rates. First, the steady-state energy release rate for interfacial delamination is linearly proportional to the TSV diameter, which may set an upper bound for the via diameter ($D_f < D_{\max}$) to avoid interfacial delamination. Second, the energy release rate is proportional to the square of the thermal mismatch strain, $\varepsilon_T = \left(\alpha_f - \alpha_m\right)\Delta T$. Thus the delamination driving force can be reduced by either using TSV materials with smaller thermal expansion mismatch or by reducing the thermal loads (ΔT) by optimizing the fabrication processes. Third, the energy release rate for interfacial delamination increases with the elastic modulus of the TSV material; however, the effect is less prominent than that of the thermal expansion mismatch. Finally, a

comparison between (Eq. 4.5) and (Eq. 4.12) indicates that, with the same magnitude for the thermal load (ΔT), the driving force for interfacial delamination under cooling is about twice of that under heating, a result that can be attributed to the presence of the tensile radial stress (σ_r) across the interface (opening mode) for the case of cooling.

4.2 EFFECTS OF CRACK LENGTH AND WAFER THICKNESS

For a finite-sized TSV structure with a finite-length interfacial crack, the energy release rate depends on both the crack length and the wafer thickness. Fig. 4.2 shows the energy release rate as a function of the crack length for different TSV diameters with a wafer thickness H=300 μm.

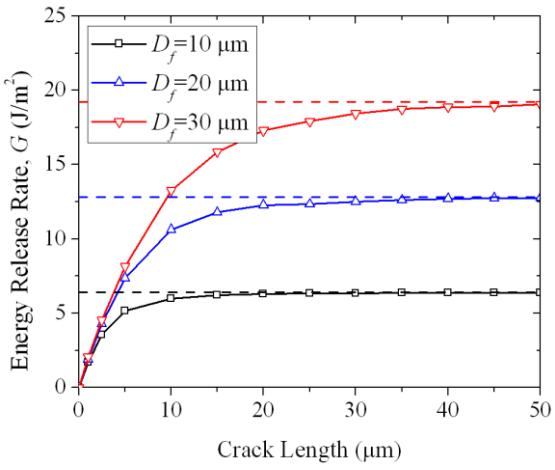


Figure 4.2: Effect of crack length on the energy release rate for interfacial delamination of TSVs (H = 300 μm and ΔT = –250 °C).

A FEA model of the TSV structure is constructed for each via diameter, and the energy release rates are calculated by the method of J-integral in ABAQUS. The material properties for the via and the substrate are taken as those of Cu and Si in Table 3.1. As expected, the energy release rate increases with the crack length and approaches the

steady-state solution when the crack length is about 2-3 times the via diameter. By equating the energy release rate with the interfacial adhesion energy, i.e., $G(a_c)=\Gamma$, a critical crack length (a_c) may be determined, beyond which the delamination crack grows unstably [117]. For a conservative design, one may require $G_{SS} \le \Gamma$ so that all cracks remain stable under the prescribed thermal load.

To illustrate the effect of wafer thickness, Fig. 4.3 shows the energy release rate as a function of the crack length for different wafer thicknesses, with the same via diameter and thermal load. For a relatively thin wafer, the energy release rate for interfacial delamination reaches a maximum and then decreases as the crack length increases, approaching the opposite side of the wafer. The maximum energy release rate decreases as the wafer thickness decreases. Therefore, the interfacial reliability of TSVs may be improved by using thinner wafers, although other effects such as wafer handling and Si cracking may compromise the overall reliability with the reduction of the wafer thickness.

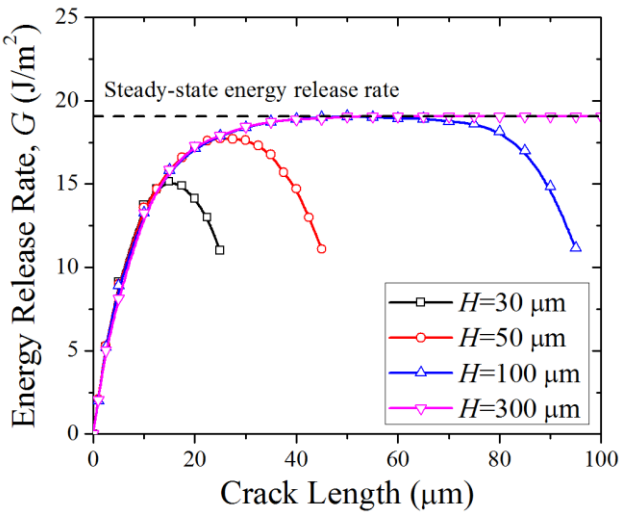


Figure 4.3: Effect of wafer thickness on the energy release rate for interfacial delamination of TSVs ($D_f = 30\,\mu m$ and $\Delta T = -250\,^{\circ}C$).

4.3 COHESIVE ZONE MODELING FOR INTERFACIAL FAILURE

4.3.1 A cohesive zone model (CZM)

Cohesive zone models (CZMs) have been widely employed to study the failure processes including nucleation and growth of interfacial cracks [118-121]. By the approach of CZM, the constitutive behavior of an interface is described by a nonlinear traction-separation law. Various traction-separation laws have been used, such as the perfect plasticity model [122], smooth nonlinear model [123], trapezoidal model [124], and bilinear or triangular model [125]. In the present study, the bilinear traction-separation law (Fig. 4.4) is employed.

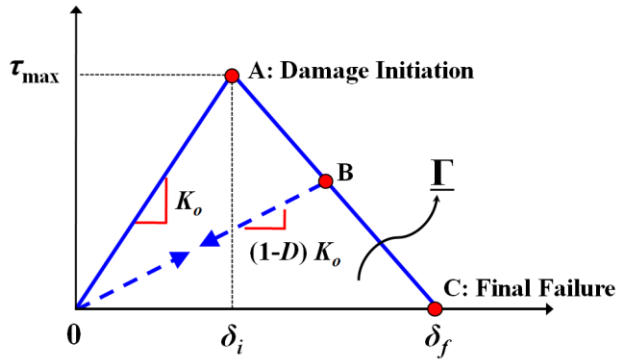


Figure 4.4: The bilinear traction-separation law.

Assuming a mode-II delamination crack, the shear traction at the interface is related to the separation displacement across the interface in the tangential direction. Starting from an intact interface, the shear traction first increases linearly with the tangential separation, with an initial stiffness K_0. At a critical separation, the shear traction reaches its maximum, τ_{max}, after which the shear traction decreases with further separation due to damage accumulation at the interface. Eventually, the shear traction becomes zero at another critical separation, δ_f, after which the traction remains zero as

the interface has been fractured. The total work done to fracture the interface is the fracture energy or interface toughness, represented by the area under the traction-separation curve, namely, $\Gamma = \frac{1}{2}\tau_{\max}\delta_f$.

The bilinear traction-separation law assumes a linear elastic behavior before the tangential separation reaches the first critical value, $\delta_i = \tau_{\max} / K_0$. For $\delta_i < \delta < \delta_f$, a damage variable, D, is defined to describe the damage evolution at the interface through the concept of elastic stiffness degradation [126],

$$D = \frac{\delta_f(\delta_{\max} - \delta_i)}{\delta_{\max}(\delta_f - \delta_i)}, \tag{4.13}$$

where $\delta_{\max}$ refers to the maximum separation attained during the loading history. The damage variable evolves from 0 at point A to 1 at point C in Fig. 4.4. In between, the interface element is partly damaged ($0 < D < 1$), and the shear traction is related to the tangential separation as

$$\tau = (1-D)K_o\delta. \tag{4.14}$$

Combining Eqs. (4.13) and (4.14) gives that the shear traction decreases linearly with the displacement δ for $\delta_i \le \delta \le \delta_f$:

$$\tau = \tau_{\max}\frac{\delta_f - \delta}{\delta_f - \delta_i}. \tag{4.15}$$

During unloading, $\delta_{\max}$ remains as a constant, and so does D. Therefore, the shear traction decreases linearly as the separation decreases, with the slope $K = (1-D)K_o$, as illustrated by the dashed line in Fig. 4.4. The damage is assumed to be irrecoverable.

4.3.2 A shear-lag model for TSV

A classical shear-lag model [127, 128] is employed as an analytic approach to predict initiation and propagation of the interfacial cracks in TSV structures. As illustrated in Fig. 4.1, the interfacial cracking modes are different in the heating and cooling processes. Here, the focus is on a TSV structure with a positive thermal load ($\Delta T > 0$), for which the interfacial fracture is in a pure shearing mode. Consider a TSV structure as shown in Fig. 4.5. The wafer thickness is *H*, and the via diameter is D_f. By symmetry, only half of the wafer is considered, with the coordinate ξ measured from the mid-plane. The interface between the via and Si may be divided into three regions: intact (I), cohesive (II), and debonded (III). l_1 is the distance from the mid-plane to the boundary between Region I and Region II, and l_2 is the distance from the mid-plane to the boundary between Region II and Region III. Starting from an intact interface, we have $l_1 = l_2 = H/2$. As ΔT increases, a cohesive region first emerges from the surface, so that $l_1 < l_2 = H/2$. At a critical temperature, an interfacial crack with fully debonded interface region is nucleated, so that $l_1 < l_2 < H/2$. Subsequently, the interfacial crack grows, as both l_1 and l_2 decreases.

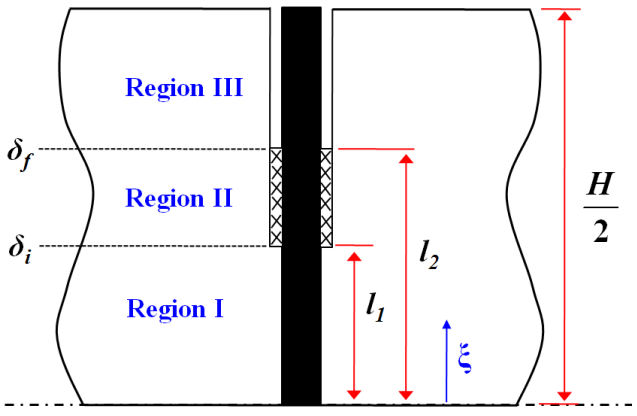


Figure 4.5: Schematic of a symmetric shear-lag model.

By the shear-lag model, the via is assumed to be subject to uniaxial stress in the axial direction, with the axial stress related to the axial displacement as

$$\sigma_f = E_f \left(\frac{du_f}{d\xi} - \alpha_f \Delta T \right). \tag{4.16}$$

By the equilibrium condition, the shear traction at the interface is

$$\tau = \frac{D_f}{4} \frac{d\sigma_f}{d\xi}. \tag{4.17}$$

By the cohesive zone model, the shear traction is related to the tangential separation by Eq. (4.14), with the damage variable D taking different values in the three regions. The tangential separation at the interface is

$$\delta = u_f - u_s = u_f - \xi \alpha_s \Delta T. \tag{4.18}$$

Combining Eqs. (4.16)-(4.18) leads to a single equation for the tangential separation:

$$\frac{E_f D_f}{4} \frac{d^2\delta}{d\xi^2} = \tau(\delta), \tag{4.19}$$

where the right-hand side is given by the traction-separation relation of the interface. The boundary conditions include: (1) $\sigma_f = 0$ at $\xi = H/2$, and (2) $u_f = 0$ at $\xi = 0$. In the following, the problem is solved analytically in three stages.

Stage I: Intact interface

In this stage, the entire interface is intact ($D = 0$). Thus, the shear traction is linearly related to the separation, namely

$$\tau = K_0 \delta. \tag{4.20}$$

Inserting (4.20) into (4.19) leads to

$$\frac{d^2\delta}{d^2\xi} = \frac{4K_0}{E_f D_f}\delta . \tag{4.21}$$

Solving (4.21) with the boundary conditions, we obtain

$$\delta = \frac{\lambda\left(\alpha_f - \alpha_s\right)\Delta T}{\cosh\left(\frac{H}{2\lambda}\right)}\sinh\left(\frac{\xi}{\lambda}\right), \tag{4.22}$$

where $\lambda = \sqrt{\frac{E_f D_f}{4K_o}}$ is a length scale. Correspondingly, the axial stress in the via is

$$\sigma_f = E_f\left(\alpha_f - \alpha_s\right)\Delta T\left[\frac{\cosh\left(\frac{\xi}{\lambda}\right)}{\cosh\left(\frac{H}{2\lambda}\right)} - 1\right]. \tag{4.23}$$

For the interface to be intact, the maximum separation at $\xi = H/2$ must be less than δ_i. Thus, the critical temperature for damage initiation at the interface is

$$\Delta T_{c1} = \frac{\delta_i}{\lambda\left(\alpha_f - \alpha_s\right)}\coth\left(\frac{H}{2\lambda}\right). \tag{4.24}$$

Stage II: Partially damaged interface with Regions I and II

When $\Delta T > \Delta T_{c1}$, a cohesive region emerge at the interface for $l_1 < \xi < H/2$. At $\xi = l_1$, the tangential separation $\delta = \delta_i$. Thus, in Region I ($0 < \xi < l$), the tangential separation is obtained by solving Eq. (4.21) with the boundary condition, namely

$$\delta = \frac{\sinh\left(\frac{\xi}{\lambda}\right)}{\sinh\left(\frac{l_1}{\lambda}\right)}\delta_i . \tag{4.25}$$

Correspondingly, the axial stress in the via is

$$\sigma_f = E_f \left[\frac{\cosh\left(\frac{\xi}{\lambda}\right)}{\sinh\left(\frac{l_1}{\lambda}\right)} \frac{\delta_i}{\lambda} - \left(\alpha_f - \alpha_s\right)\Delta T \right] \quad \text{for} \quad 0 < \xi < l_1 . \tag{4.26}$$

In Region II ($l_1 < \xi < H/2$), the interface is partially damaged, with the damage variable, D, by Eq. (4.13). The shear stress at the interface is given by Eq. (4.15). Inserting Eq. (4.15) into (4.19), we obtain another O.D.E. for Region II:

$$\frac{E_f D_f}{4} \frac{d^2\delta}{d\xi^2} = -A(\delta - \delta_f) . \tag{4.27}$$

where $A = \dfrac{\tau_{\max}}{\delta_f - \delta_i}$.

The O.D.E (Eq. 4.27) is solved with the following boundary conditions: (1) $\sigma_f = 0$ at $\xi = H/2$, and (2) $\delta = \delta_i$ at $\xi = l_1$. Moreover, to determine l_1, the continuity condition is applied for the axial stress in the via, i.e., $\sigma_f\left(\xi = l_1^+\right) = \sigma_f\left(\xi = l_1^-\right)$. With these conditions, we obtain that

$$\delta = \delta_f + C_1 a \sin\left(\frac{\xi - l_1}{a}\right) + C_2 a \cos\left(\frac{\xi - l_1}{a}\right) \qquad (l_1 \le \xi \le H/2) . \tag{4.28}$$

where $C_1 = \dfrac{\delta_i}{\lambda}\coth\left(\dfrac{l_1}{\lambda}\right)$, $C_2 = \dfrac{\delta_i - \delta_f}{a}$, and $a = \sqrt{\dfrac{E_f D_f}{4A}}$ is another length scale. The length l_1 is given implicitly by the following equation:

$$C_1 \cos\left(\frac{H/2 - l_1}{a}\right) - C_2 \sin\left(\frac{H/2 - l_1}{a}\right) = \left(\alpha_f - \alpha_s\right)\Delta T . \tag{4.29}$$

As ΔT increases ($\Delta T > \Delta T_{c1}$), l_1 decreases and the cohesive zone size ($H/2 - l_1$) increases. Eventually, at another critical temperature, an interfacial crack is initiated with a fully debonded region (Region III) emerging from the surface. This critical temperature is predicted by setting the maximum separation at $\xi = H/2$ to be δ_f, namely

$$C_1 \sin\left(\frac{H/2-l_1}{a}\right)+C_2\cos\left(\frac{H/2-l_1}{a}\right)=0\,. \tag{4.30}$$

Combine this with the equation for l_1 in (4.29), we obtain

$$\left(\alpha_f-\alpha_s\right)\Delta T_{c2}\sin\left(\frac{H/2-l_1\left(\Delta T_{c2}\right)}{a}\right)=\frac{\delta_f-\delta_i}{a}\,, \tag{4.31}$$

which can be solved to determine ΔT_{c2}.

Stage III: Partially fractured interface with Regions I, II, and III

When $\Delta T>\Delta T_{c2}$, an interfacial crack would grow along with a cohesive region, as illustrated in Fig. 4.5. In Region I ($0<\xi<l_1$), the tangential separation and the axial stress in the via take the same form as for Stage II. In Region II ($l_1<\xi<l_2$), however, the boundary conditions are different from Stage II. By the continuity condition, we have (1) $\sigma_f=0$ at $\xi=l_2$, and (2) $\delta=\delta_f$ at $\xi=l_2$. The tangential separation in Region II takes a similar form:

$$\delta=\delta_f+C_1 a\sin\left(\frac{\xi-l_1}{a}\right)+C_2 a\cos\left(\frac{\xi-l_1}{a}\right)\qquad (\,l_1\le\xi\le l_2\,)\,. \tag{4.32}$$

Meanwhile, the continuity conditions at $\xi=l_2$ leads to

$$C_1\cos\left(\frac{l_2-l_1}{a}\right)-C_2\sin\left(\frac{l_2-l_1}{a}\right)=\left(\alpha_f-\alpha_s\right)\Delta T\,. \tag{4.33}$$

$$C_1\sin\left(\frac{l_2-l_1}{a}\right)+C_2\cos\left(\frac{l_2-l_1}{a}\right)=0\,. \tag{4.34}$$

which can be solved simultaneously to determine l_1 and l_2, both decreasing with ΔT.

In Region III ($l_2<\xi<H/2$), the damage variable, $D=1$, and the shear traction $\tau=0$. Thus, this part of the via is not constrained by the Si substrate and deforms freely by thermal expansion. By Eq. (4.19), the tangential separation increases linearly with ξ, i.e.,

$$\delta = \delta_f + (\xi - l_2)(\alpha_f - \alpha_s)\Delta T\,. \tag{4.35}$$

Correspondingly, the axial stress in the via is zero for $l_2 < \xi < H/2$.

4.3.3 Critical temperatures for debonding

Two critical temperatures are predicted by the cohesive zone model for interfacial failure of the TSV. For the convenience of discussion, the physical and geometrical parameters are normalized as follows.

Temperature change: $\bar{\Delta T} = (\alpha_f - \alpha_s)\Delta T$, (4.36)

Interfacial strength: $\bar{\tau}_{\max} = \dfrac{\tau_{\max}}{E_f}$, (4.37)

Interfacial Stiffness: $\bar{K}_0 = \dfrac{K_0 D_f}{E_f}$, (4.38)

Interfacial Toughness: $\bar{\Gamma} = \dfrac{\Gamma}{E_f D_f}$, (4.39)

Via depth (aspect ratio): $\bar{H} = \dfrac{H}{D_f}$. (4.40)

The first critical temperature defines the temperature when an intact TSV structure starts to accumulate damage at the interface, forming a cohesive zone near the free surface. By (4.24), the critical temperature after normalization can be expressed as a function of three dimensionless parameters, $\bar{H}$, $\bar{\tau}_{\max}$, and $\bar{K}_0$, namely

$$\bar{\Delta T}_{c1} = \frac{2\bar{\tau}_{\max}}{\sqrt{\bar{K}_0}} \coth\left(\bar{H}\sqrt{\bar{K}_0}\right). \tag{4.41}$$

Note that the first critical temperature (for damage initiation) is independent of the interfacial toughness, but depends on the interfacial strength and the aspect ratio of the via. In the limiting case for a high aspect ratio, $\bar{H} >> 1$, we have approximately

$$\Delta\bar{T}_{c1} \approx \frac{2\bar{\tau}_{\max}}{\sqrt{\bar{K}_0}}. \tag{4.42}$$

The second critical temperature defines the temperature when an interfacial crack starts to nucleate from the cohesive zone with a fully debonded region. By Eq. (4.31), the critical temperature is given implicitly. After normalization, it can be expressed as a function of four dimensionless parameters, $\bar{H}$, $\bar{\Gamma}$, $\bar{\tau}_{\max}$, and $\bar{K}_0$, namely

$$\Delta\bar{T}_{c2} = f(\bar{\Gamma}, \bar{\tau}_{\max}, \bar{K}_0, \bar{H}). \tag{4.43}$$

Thus, the second critical temperature (for crack initiation) does depend on the interfacial toughness in addition to the other three parameters. In the limiting case for a high aspect ratio, $\bar{H} >> 1$, we have approximately

$$\Delta\bar{T}_{c2} \approx \sqrt{8\bar{\Gamma}}. \tag{4.44}$$

Similar results have been obtained previously for fiber-reinforced composites [129].

As an example, the calculations in this section used the following properties for the TSV structure: the elastic modulus of via, $E_f = 110\,\text{GPa}$, the thermal expansion mismatch, $\alpha_f - \alpha_s = 14.7\ \text{ppm/}^{\text{o}}\text{C}$, the interfacial strength, $\tau_{\max} = 150\,\text{MPa}$, the interfacial toughness, $\Gamma = 2.0\ \text{J/m}^2$, and the initial separation, $\delta_i = 10$ nm. In addition, the geometrical dimensions such as the TSV height, H = 60 μm, and via diameter, $D_f = 6\,\mu\text{m}$, are used. As defined by Eqs. (4.36)~(4.40), the normalized parameters are:

$$\begin{aligned} &\bar{\Gamma} = 3\times10^{-6} \\ &\bar{\tau}_{\max} = 0.0013 \\ &\bar{K}_0 = 0.81 \\ &\bar{H} = 10 \end{aligned}. \tag{4.45}$$

The two critical temperatures are plotted in Fig. 4.6 as a function of the aspect ratio, $\bar{H}$. Both the critical temperatures increase as $\bar{H}$ decreases for relatively small aspect ratios ($\bar{H} < 3$). For larger aspect ratios, the critical temperatures become

independent of $\bar{H}$. By the approximate solutions in (4.42) and (4.44), the critical temperatures for large aspect ratios are 196 °C for first critical temperature and 333 °C for second critical temperature, respectively.

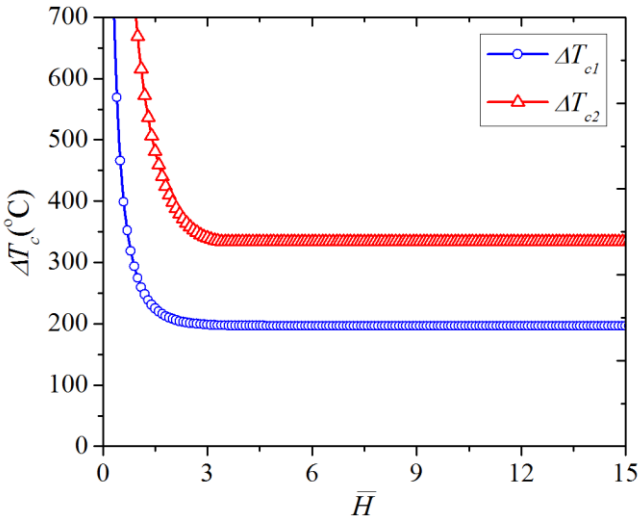
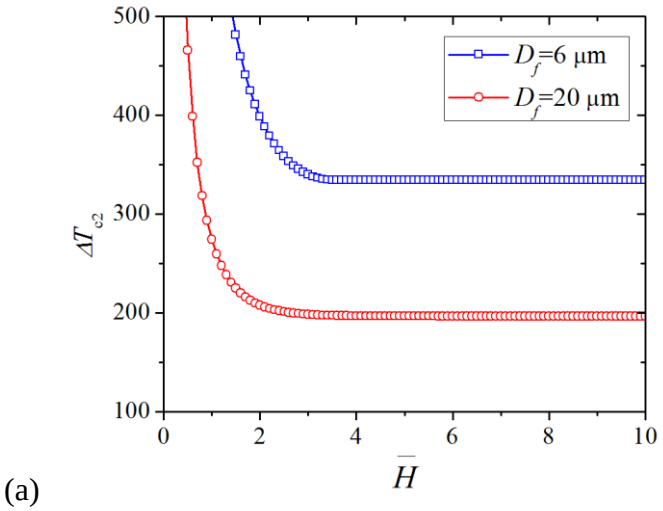


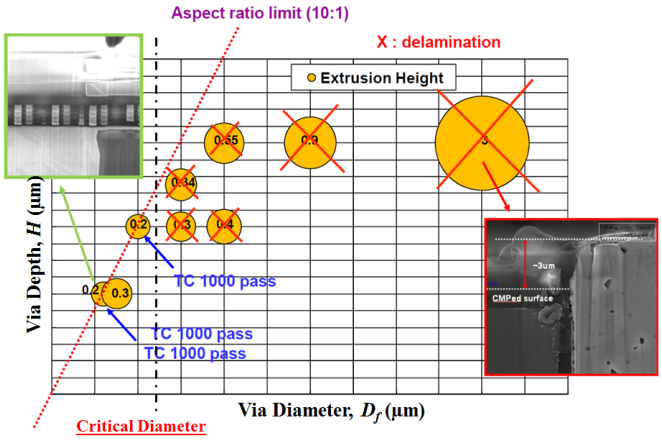
Figure 4.6: Critical temperatures for interfacial failure of the TSV structure.

It is noted that the normalized parameters, $\bar{K}_0$ and $\bar{\Gamma}$, depend on the via diameter (D_f). As the via diameter increases, $\bar{K}_0$ increases and $\bar{\Gamma}$ decreases. As a result, by (4.42) and (4.44), both the critical temperatures decrease if the aspect ratio ($\bar{H}$) remains relatively large. As shown in Fig. 4.7a, the second critical temperature decreases as the via diameter increases for all aspect ratios with a fixed interface toughness, $\Gamma = 2.0\,\text{J/m}^2$. Given a particular thermal load (e.g., $\Delta T = 300$ °C), according to Fig. 4.7a, interfacial delamination would not occur in the vias with $D_f = 6\,\mu\text{m}$, since $\Delta T < \Delta T_{c2}$ for all aspect ratios. For the vias with $D_f = 20\,\mu\text{m}$, however, interfacial delamination would occur for those with large aspect ratios ($\bar{H} > 1$), but not for those with small aspect ratios. Fig. 4.7b shows experimental data for the via extrusion due to interfacial

delamination. In this study [53], via extrusion was measured as a function of the via depth and diameter. It was found that interfacial delamination occurred only for the vias with relatively large diameters, which is consistent with the prediction by the shear-lag model in the present study.



(a)



(b)

Figure 4.7: (a) Effect of via diameter on the second critical temperature; (b) Experimental observation of via extrusion and interfacial delamination for different via diameters and depths (Source: Samsung [53]).

Furthermore, the effects of interfacial properties, such as toughness and strength on the critical temperatures, were investigated. Fig 4.8 shows that the second critical temperature becomes higher as the interfacial toughness increases. The first critical temperature is independent of the toughness.

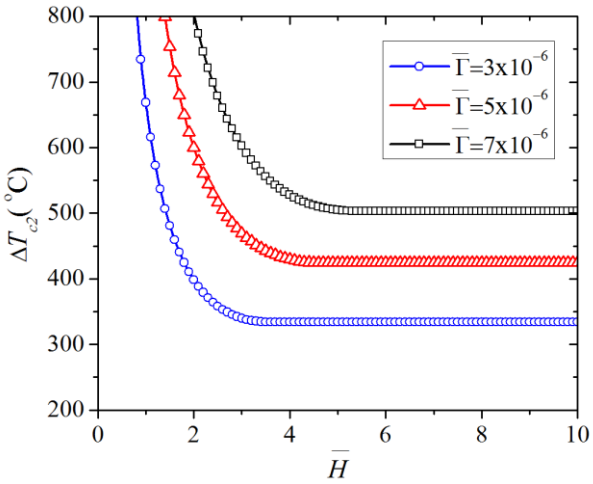


Figure 4.8: Effect of interfacial toughness on the critical temperature ($\bar{\tau}_{\max} = 0.0013$ and $\bar{K}_0 = 0.81$).

Next, the effect of interfacial strength on the critical temperature is shown in Fig. 4.9. The first critical temperature increases with increasing interfacial strength. However, the second critical temperature shows an opposite trend. With the same interfacial toughness, the second critical temperatures for different interfacial strengths converge to the same value for sufficiently large aspect ratios ($\bar{H} >> 1$), as predicted by Eq. (4.44). For relatively small aspect ratios, the second critical temperature depends on the interfacial strength. By the bilinear traction-separation relation (Fig. 4.4), for the same toughness, a higher strength results in a smaller critical separation at final failure. The size of the cohesive zone decreases with increasing strength. If the cohesive zone size is

small compared to the via depth (small-scale bridging), the result is independent of the strength. However, when the cohesive zone size is comparable to the depth (large-scale bridging), the second critical temperature decreases with decreasing cohesive zone size. Therefore, in general, both the strength and the toughness of the interface are needed to determine the interfacial reliability in the TSV structures.

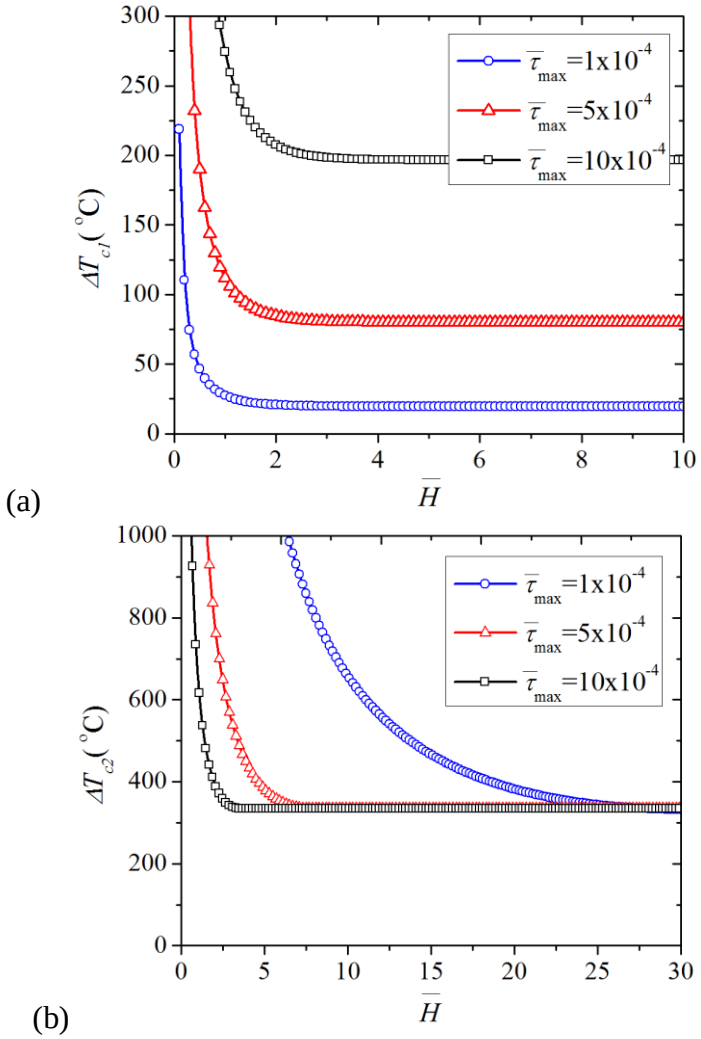


Figure 4.9: Effect of interfacial strength on the critical temperatures ($\bar{\Gamma} = 3\times10^{-6}$ and $\bar{K}_0 = 0.81$): (a) First critical temperature; (b) Second critical temperature.

4.3.4 Via extrusion

The tangential separation displacement at the wafer surface may be observed as via extrusion. By the combination of the cohesive zone model and the shear-lag model, the separation displacement at the surface ($\xi = H/2$) is determined as a function of the thermal load (ΔT). In Stage I ($\Delta T < \Delta T_{c1}$), by Eq. (4.17), the extrusion displacement is

$$\hat{\delta} = \lambda\left(\alpha_f - \alpha_s\right)\Delta T \tanh\left(\frac{H}{2\lambda}\right). \tag{4.46}$$

In this stage, since the interface remain intact, the extrusion displacement depends on the elastic properties of the via and interface only, which is relatively small ($\hat{\delta} < \delta_i$). In Stage II ($\Delta T_{c1} < \Delta T < \Delta T_{c2}$), the extrusion displacement at the surface is given by

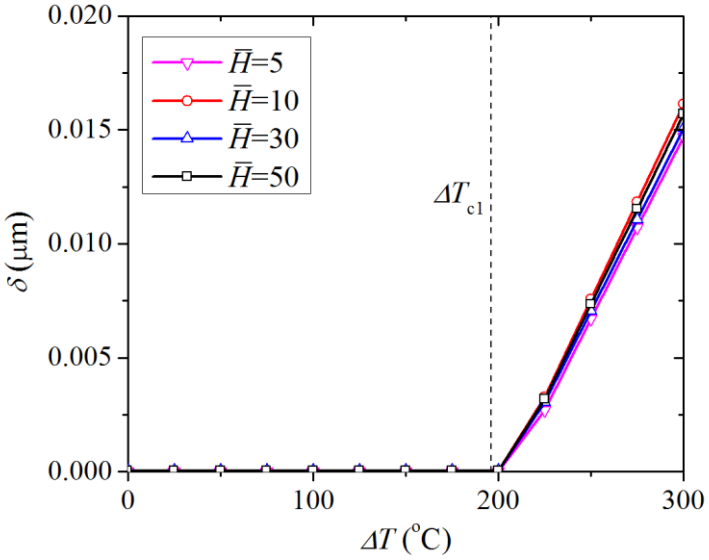
$$\hat{\delta} = \delta_f - \left(\delta_f - \delta_i\right)\cos\left(\frac{H/2 - l_1}{a}\right) + \frac{\delta_i a}{\lambda}\coth\left(\frac{l_1}{\lambda}\right)\sin\left(\frac{H/2 - l_1}{a}\right). \tag{4.47}$$

where l_1 is a function of ΔT by Eq. (4.29). Finally, in Stage III ($\Delta T > \Delta T_{c2}$), the extrusion displacement is

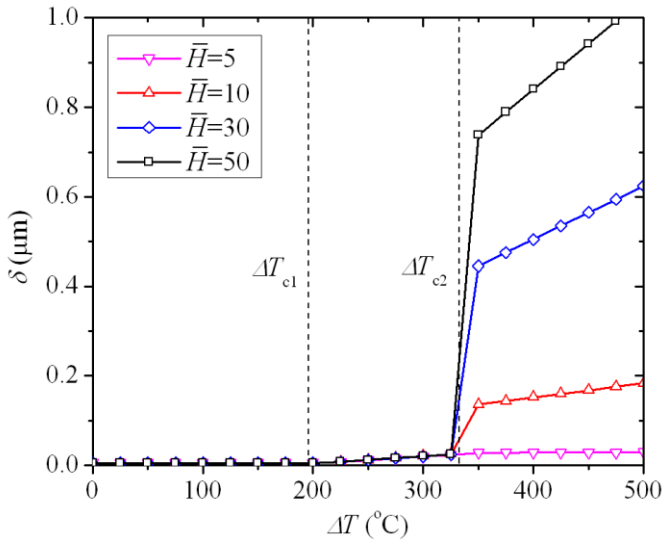
$$\hat{\delta} = \delta_f + \left(\frac{H}{2} - l_2\right)\left(\alpha_f - \alpha_s\right)\Delta T\,. \tag{4.48}$$

where l_2 is a function of ΔT by solving Eqs. (4.33) and (4.34) simultaneously.

Fig. 4.10 plots the extrusion displacement as a function of the thermal load. The extrusion displacement increases linearly during Stage I. At the first critical temperature, the extrusion displacement kinks up to increase more rapidly in Stage II. At the second critical temperature, the extrusion displacement increases abruptly due to crack nucleation at the interface. Furthermore, the extrusion displacement increases with the normalized via height, which suggests that wafer thinning (or reduction of the TSV height) can help reduce via extrusion. Similar trends were observed by Samsung [53] (Fig. 4.11), even though specific temperatures were not provided in the latter paper.

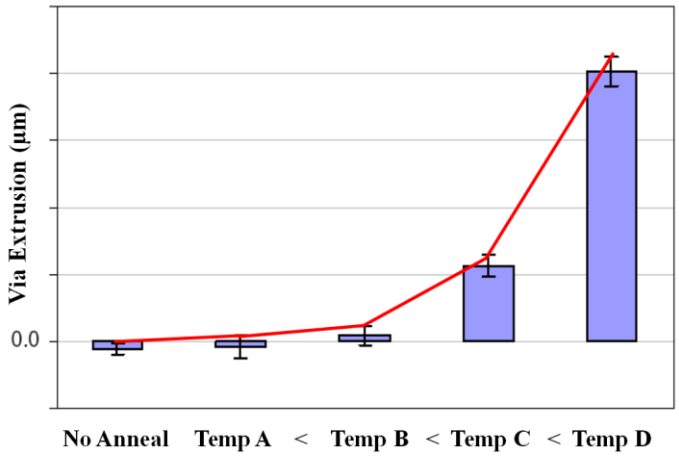


(a)



(b)

Figure 4.10: (a) Via extrusion displacement after first critical temperature; (b) Via extrusion after second critical temperature by the shear-lag model.



(b)

Figure 4.11: Via extrusion observed for various 'unspecified' temperatures (Source: Samsung [53]).

4.3.5 Finite Element Analysis (FEA)

Finite element models were developed to simulate the initiation and growth of interfacial delamination in the TSV structure. All the materials are assumed to be linear elastic, while the interface between the via and Si is modeled by cohesive elements with the bilinear traction-separation relation. In the present research, an axi-symmetric FEA model was used for computational efficiency. For the calculation, the material properties listed in Eq. 4.45 were used. The via and Si parts were meshed with 0.1×0.06 µm axisymmetric element (CAX4R), while the interface was modeled with a layer of 0.02×0.06 µm cohesive element (COHAX4). Fig. 4.12 describes the debonding process with increasing temperature. As expected from the analytic solution, the via extrusion dramatically increases after the second critical temperature (Fig. 4.12c).

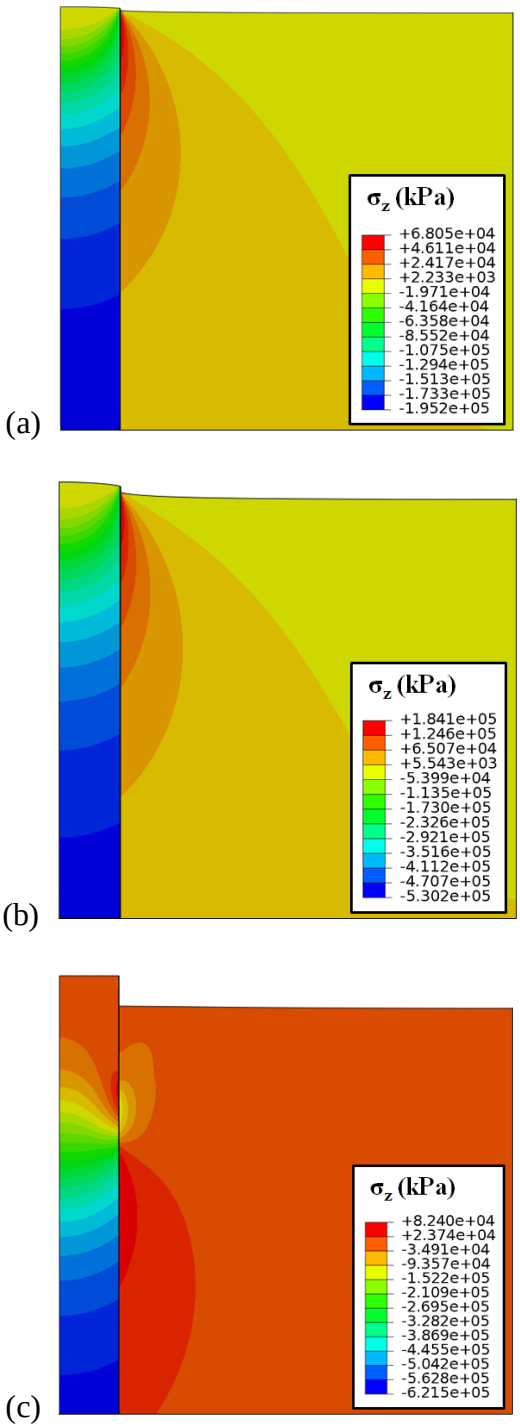
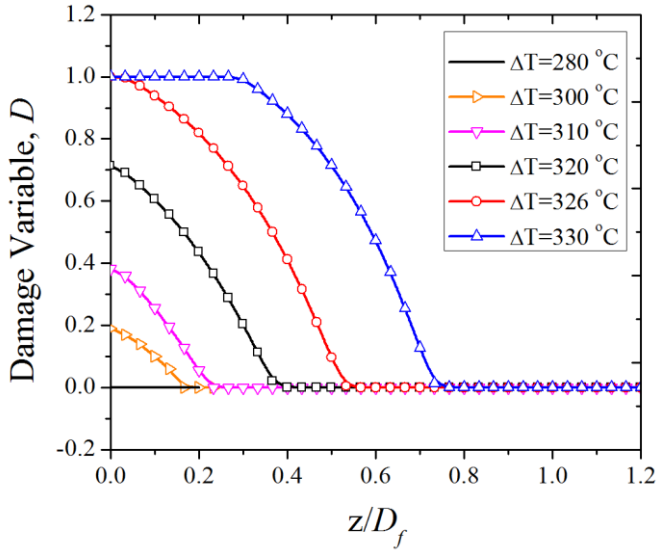


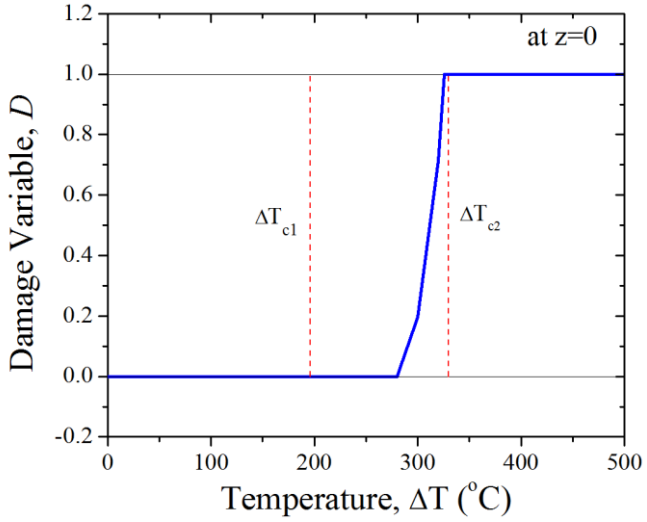
Figure 4.12: Simulation of via extrusion during heating process: (a) $\Delta T = 100\,^{o}\mathrm{C}$; (b) $\Delta T = 280\,^{o}\mathrm{C}$; (c) $\Delta T = 350\,^{o}\mathrm{C}$.

Fig. 4.13a plots the interfacial damage variable, D, along the depth (z/D_f) from the FEA model with a fixed height ($H/D_f=10$) for different thermal loads. The damage variable remains zero everywhere until the first critical temperature is reached. As predicted by the shear-lag model, the interfacial behavior follows the linear elastic traction-separation relation in Stage I ($\Delta T<\Delta T_{c1}$). For $\Delta T>\Delta T_{c1}$, a damage zone emerges with $0<D<1$ and grows along the interface. The maximum damage variable at the surface/interface junction ($z=0$) is less than 1 for $\Delta T<326\,^{o}$C. At the second critical temperature ($\Delta T_{c2}=326\,^{o}$C), a crack is nucleated with $D=1$ at the surface/interface junction. Subsequently, the crack grows along the interface with a steady-state damage zone ahead of the crack tip.

Figure 4.13b plots the interfacial damage variable at the surface/interface junction ($z=0$) as a function of the temperature change, which shows clearly the two critical temperatures. For comparison, the critical temperatures predicted by the shear-lag model are indicated by the vertical dashed lines in Fig. 4.13b. Apparently, the first critical temperature is ~200^{o}C according to the analytic solution, which is lower than the FEA calculation (~280^{o}C). On the other hand, the second critical temperature predicted by the shear-lag model is in good agreement with the FEA result. The shear-lag model predicts the second critical temperature to be 335^{o}C at $H/D_f=10$, while the FEA model predicts it to be 326 ^{o}C. Moreover, Figure 4.14 compares the via extrusion displacement obtained from the FEA model with the prediction by the shear-lag model. The differences between the two models can be attributed to the non-uniform stress distribution in the via as shown in Fig. 4.12.



(a)



(b)

Figure 4.13: Damage evolution with increasing temperature, ΔT : (a) Damage variable vs. depth; (b) Damage variable at $z = 0$ vs. temperature (the red dashed lines indicate the two critical temperatures obtained from the shear-lag model).

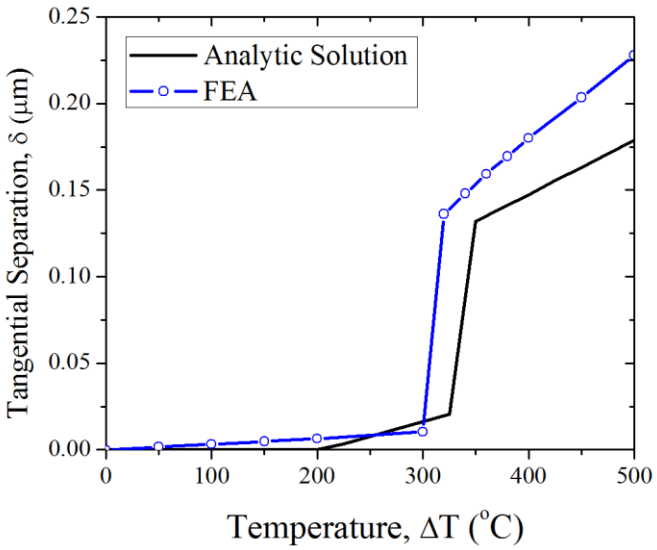


Figure 4.14: Via extrusion displacement with increasing temperature.

4.4 SUMMARY

As a study on the interfacial reliability of TSVs, the energy release rate for interfacial delamination in a TSV structure is evaluated under both cooling and heating conditions. An analytical solution is obtained for the steady-state energy release rate as the upper bound for the interfacial fracture driving force, while the effects of crack length and wafer thickness are evaluated numerically by FEA models. Moreover, by combining a cohesive zone model with a shear-lag model, an analytical approach is developed to predict initiation and growth of interfacial delamination in the TSV structure. Two critical temperatures are predicted for damage initiation and fracture initiation, respectively. It is found that via extrusion increases significantly beyond the second critical temperature. The dependence of the critical temperatures on the material/interfacial properties as well as the via size (diameter and height) is discussed. Finite element models with cohesive interface elements are employed to numerically

simulate the process of interfacial delamination, in comparison with the analytical approach.

Chapter 5

Structural Designs and Materials for TSVs

Different structural designs of TSV structures have been considered and tested, in search for an optimum design for both performance and reliability. As illustrated in Fig. 2.1, these include fully-filled TSVs by Hynix [55], Fujitsu and Novellus, TSVs with a thick barrier layer by Hynix, TSVs with nail-head by Intel, Qualcomm, and Freescale, annular TSVs by Samsung [53]. Furthermore, various materials (e.g., W and Ni) have been suggested as alternative via metals in place of Cu. In this Chapter, the effects of structural designs and the variation of the constituent materials on TSV reliability are investigated.

5.1 FULLY-FILLED TSV: EFFECT OF VIA MATERIALS

Interfacial delamination of a fully filled TSV (Fig. 2.1a) has been studied in Chapter 4. In particular, the steady-state energy release rate for the interfacial crack growth is obtained analytically for both cooling and heating processes, setting an upper bound for the fracture driving force. The effect of different via materials on the interfacial fracture driving force for the fully filled TSVs is evaluated using the thermo-mechanical properties listed in Table 5.1. The steady-state energy release rates for the four TSV materials were compared in Fig. 5.1 under both cooling ($\Delta T = -250$ ℃) and heating ($\Delta T = 250$ ℃) conditions using Eq. (4.4) and (4.11), with a fixed TSV diameter of 30 μm. The comparison in Fig. 5.1 indicates that, with the same magnitude of the thermal load (ΔT), the driving force for interfacial delamination under cooling is about twice of that under heating, a result that can be attributed to the presence of the tensile radial stress (σ_r) across the interface (opening mode) for the case of cooling. Compared to Cu, Al has

a lower Young's modulus but a larger mismatch in CTE with Si. Consequently, the driving force for interfacial delamination is higher for Al under the same thermal load. In contrast, Ni has a higher Young's modulus than Cu but a lower thermal mismatch, resulting in a lower driving force for delamination. Despite the highest Young's modulus, W has a very small CTE mismatch with Si, and thus the delamination driving force is significantly lower than for the Cu TSV. This renders W a particularly attractive material for TSV applications from the interfacial reliability perspective.

Table 5.1: Thermomechanical properties of the materials used in the present study.

Material	CTE (ppm/^{o}C)	Young's Modulus (GPa)	Poisson's ratio
Si	2.3	130	0.28
Cu	17	110	0.35
Al	20	70	0.35
Ni	13	207	0.31
W	4.4	400	0.28
BCB	40	3.0	0.34

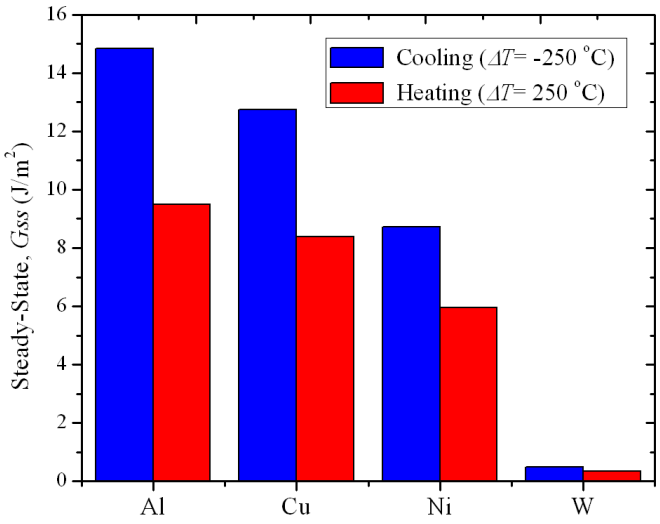


Figure 5.1: Comparison of the steady-state energy release rates for interfacial delamination in TSV structures using different via materials, under the same thermal load for cooling and heating ($D_f = 30\,\mu\text{m}$).

To evaluate the material effect on the TSV reliability, other factors have to be considered in addition to the fracture driving force [130]. In particular, these include the processing temperature for the specific metal, the TSV diameter and the interfacial adhesion energy. Since different TSV materials will require processes with different thermal loads, this can affect the delamination driving force, which is proportional to the square of the thermal mismatch strain. Among the four metals considered here, the CVD process for W deposition has the highest temperature at around 400°C, and thus the highest thermal load. This is balanced by the relatively small diameter for the W-TSV. For each TSV material, the energy release rate has to be compared with the specific interfacial adhesion energy, i.e., $G(a_c) = \Gamma$, to determine a critical crack length (a_c), beyond which the delamination crack grows unstably. The interfacial adhesion varies with the TSV material and may be enhanced by using thin adhesive barrier layers between the TSV and Si [131]. In addition, plastic yielding of the via material could

partially relax the thermal stress induced in the via and the Si, thus reducing the fracture driving force. Moreover, the energy dissipation during plastic deformation could contribute to the enhancement of overall fracture energy [132]. Therefore, the interfacial reliability may be improved by plasticity in the via. However, plastic deformation is irrecoverable and could lead to other reliability issues such as dislocations, stress voiding and fatigue. As shown in Chapter 3, without interfacial delamination, plastic deformation in the via could lead to significant via extrusion. Further studies are required to understand the effect of plasticity on thermo-mechanical reliability of TSVs.

5.2 ANNULAR TSV

5.2.1 Energy release rate

The annular TSV structure (Fig. 2.1b) is an attractive solution to reduce the impact of the thermal mismatch on interfacial reliability by means of reducing the metal volume. With the traction-free boundary condition on the inner surface of the annular TSV, the stress distribution in the via becomes non-uniform, different from that in a fully filled circular TSV. The 2-D solutions for the stress distribution in the annular TSV give the following stress components:

$$\sigma_r = \frac{-E_f \varepsilon_T}{1-2\nu_f+\eta^2+\left(1-\eta^2\right)\dfrac{1+\nu_m}{1+\nu_f}\dfrac{E_f}{E_m}}\left[1-\left(\frac{D_i}{2r}\right)^2\right], \tag{5.1}$$

$$\sigma_\theta = \frac{-E_f \varepsilon_T}{1-2\nu_f+\eta^2+\left(1-\eta^2\right)\dfrac{1+\nu_m}{1+\nu_f}\dfrac{E_f}{E_m}}\left[1+\left(\frac{D_i}{2r}\right)^2\right], \tag{5.2}$$

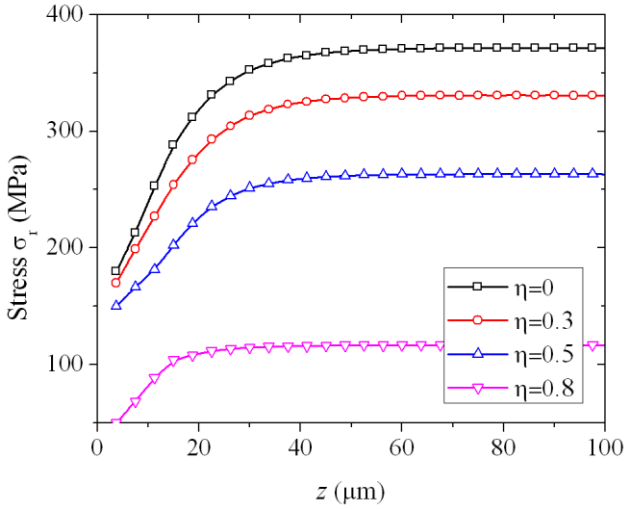
$$\sigma_z = -E_f \varepsilon_T \left[\frac{\left(1 + \frac{1+\nu_m}{1+\nu_f}\frac{E_f}{E_m}\right)}{1 - 2\nu_f + \eta^2 + \left(1-\eta^2\right)\frac{1+\nu_m}{1+\nu_f}\frac{E_f}{E_m}} \right], \tag{5.3}$$

where D_i is the inner diameter of the annular TSV and $\eta = \frac{D_i}{D_f}$ is the diameter ratio.

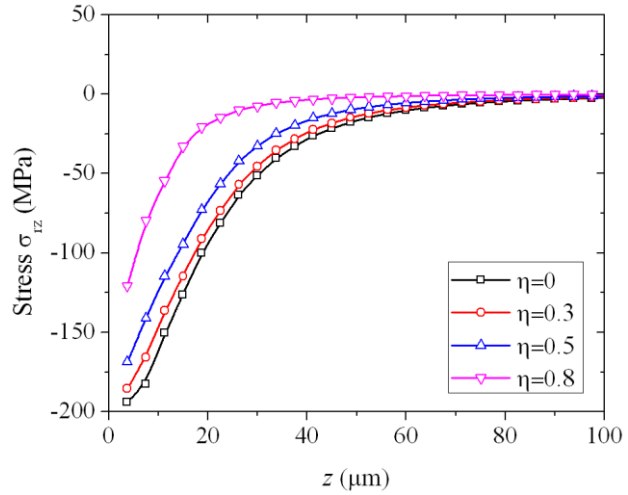
Correspondingly, the stress components in the Si are:

$$\sigma_r = -\sigma_\theta = \frac{-E_f \varepsilon_T \left(1-\eta^2\right)}{1 - 2\nu_f + \eta^2 + \left(1-\eta^2\right)\frac{1+\nu_m}{1+\nu_f}\frac{E_f}{E_m}} \left(\frac{D_f}{2r}\right)^2. \tag{5.4}$$

To obtain stress distribution at the interface, FEA was performed. Figure 5.2 shows the stress distribution at the interface ($r = D_f / 2$) along the depth (z) with $H = 300\,\mu\text{m}$. The results show apparent stress relaxation at the Cu/Si interface by introducing annular structure. As the diameter ratio, η increases by increasing the inner diameter, the radial and shear stress are reduced compared with the fully filled TSV ($\eta = 0$). In particular, the radial stress eventually reaches the 2-D solution (Eq. 5.1) at a certain depth, while all shear stresses converge to zero. The depth where the stress approaches the 2-D solution depends on several parameters such as via dimension, thermal loading, and materials, etc..



(a)



(b)

Figure 5.2: Stress distribution at the interface for annular TSVs ($D_f = 30\,\mu\text{m}$, and $\Delta T = -250$ ℃): (a) Radial stress, σ_r ; (b) Shear stress, σ_{rz} .

A steady-state energy release rate (ERR) for interfacial delamination was developed to analyze the effect of stress relaxation in annular TSVs. Based on Eqs. (5.1-4), the elastic strain energy density (per unit volume) in the TSV and Si far ahead of the crack front is, respectively,

$$U_f = E_m \varepsilon_T^2 \left(\frac{(1-\alpha^2)(1+\nu_f)(1-2\nu_f+(D_i/2r)^4)}{\left[(1-2\nu_f+\eta^2)(1-\alpha)+(1-\eta^2)(1+\alpha)\frac{1+\nu_m}{1+\nu_f}\right]^2} + \frac{1}{2}\frac{1+\alpha}{1-\alpha} \right), \tag{5.5}$$

$$U_m = E_m \varepsilon_T^2 \frac{(1+\nu_m)(1+\alpha)^2(1-\eta^2)^2}{\left((1-2\nu_f+\eta^2)(1-\alpha)+(1-\eta^2)(1+\alpha)\frac{1+\nu_m}{1+\nu_f}\right)^2} \frac{D_f^4}{(2r)^4}. \tag{5.6}$$

The release of the elastic energy per unit length of the interfacial crack is,

$$\Delta U = 2\pi \int_{D_i/2}^{D_f/2} U_f(r) r dr + 2\pi \int_{D_f/2}^{\infty} U_m(r) r dr. \tag{5.7}$$

Thus, under the cooling condition, the steady-state energy release rate for interfacial delamination is

$$G_{ss} = \frac{(1-\eta^2)E_m \varepsilon_T^2 D_f}{4} \left(\frac{(1+\nu_f)(1+\alpha)}{(1-2\nu_f+\eta^2)(1-\alpha)+(1-\eta^2)(1+\alpha)\frac{1+\nu_m}{1+\nu_f}} + \frac{1}{2}\frac{1+\alpha}{1-\alpha} \right). \tag{5.8}$$

Neglecting the elastic mismatch ($\alpha = 0$ and $\nu_f = \nu_m = \nu$), Eq. (5.8) reduces to

$$G_{ss} = \frac{(1-\eta^2)E\varepsilon_T^2 D_f}{4(1-\nu)}. \tag{5.9}$$

5.2.2 Effect of TSV materials

Figure 5.3 shows the effect of the diameter ratio of the annular TSV ($\eta = \frac{D_i}{D_f}$) on the steady-state energy release rate for Al, Cu, Ni, and W TSVs for a fixed outer diameter ($D_f = 30\,\mu\text{m}$) and the same thermal loading ($\Delta T = -250$ ℃). Clearly, the driving force for interfacial fracture decreases with increasing diameter ratio (η), suggesting improved interfacial reliability for the annular TSVs relative to the fully filled circular TSVs ($\eta = 0$) under the same thermal loading. A similar result can be obtained for the steady-state

energy release rate under heating condition ($\Delta T > 0$). The the steady-state energy release rate under heating condition is typically lower than that under cooling condition.

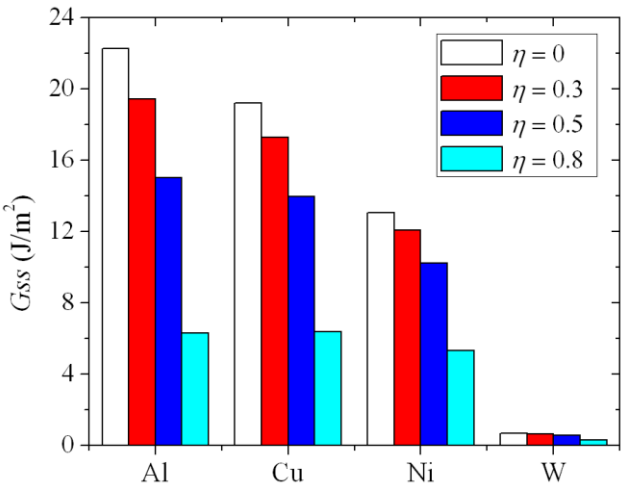


Figure 5.3: Effect of TSV materials for annular TSV on ERR ($D_f = 30$ μm and $\Delta T = -250$ ℃).

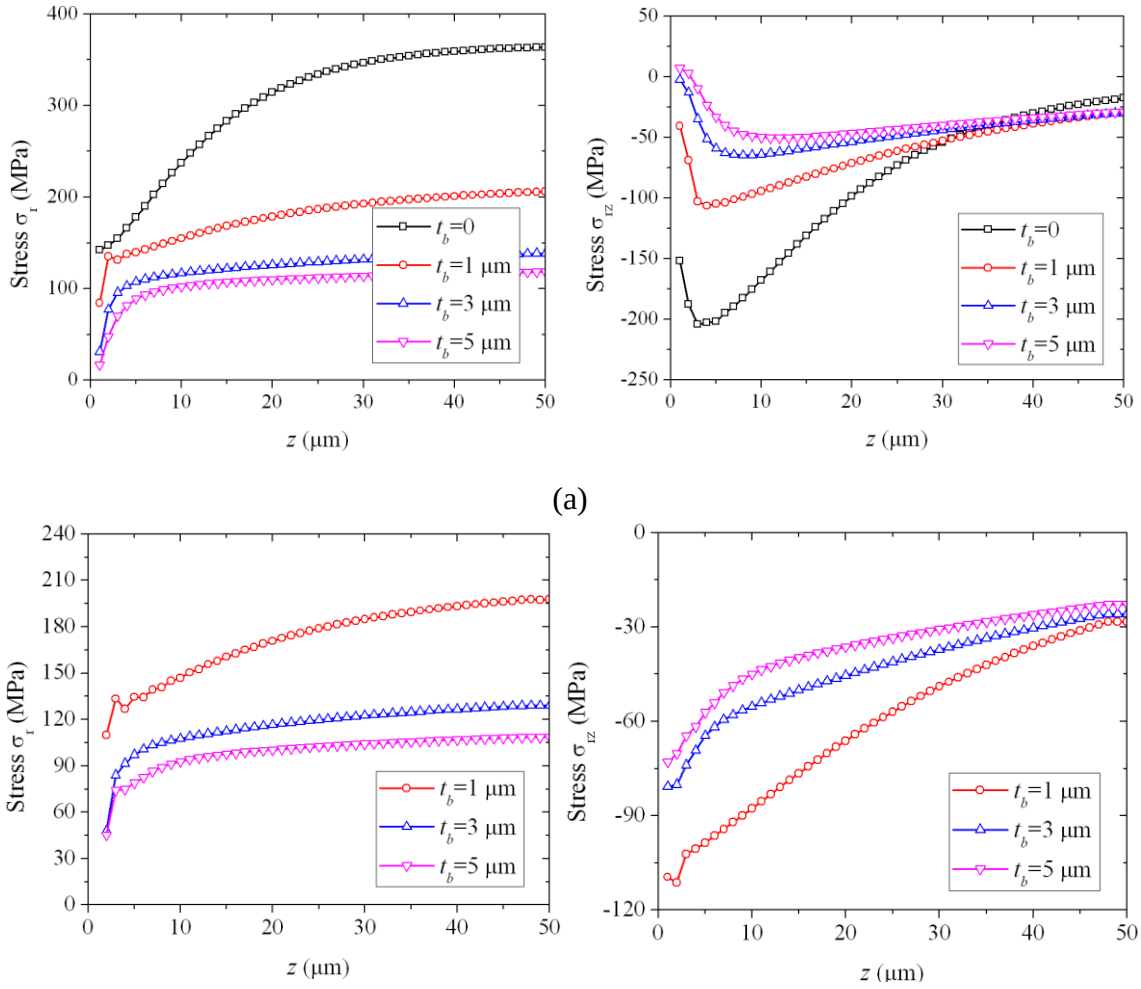
5.3 TSV WITH A DIELECTRIC BUFFER LAYER

5.3.1 Energy release rate

The study so far has considered a simplified structure with a single TSV embedded in Si. In practice, a thin barrier layer and/or a dielectric buffer layer may be needed between the TSV and Si. For example, to fabricate Cu TSVs, a dielectric and/or a barrier layer is typically deposited on the via sidewall before Cu electroplating. Similar to that in the Cu damascene interconnects, a barrier layer is usually made of metallic materials such as Ti, Ta, and their respective nitrides, TiN and TaN, with a thickness less than 0.1 μm [133-135]. While these layers provide a good anti-diffusion effect and possibly enhanced adhesion for the interface, such a thin barrier layer has little effect on the thermal stresses and the interfacial fracture driving force. This has been confirmed by

finite element analysis (FEA). Therefore, the TSV structure with thin barrier layer may be categorized simply as a fully filled TSV. The dielectric layer, on the other hand, usually made of 1~2 μm thick silicon dioxide, provides electrical insulation between Cu and Si. A typical dielectric layer can be TEOS (Tetraethyl orthosilicate) and a polymer film (Fig. 2.1c). In practice, TEOS (Tetraethyl orthosilicate) could serve as a strong insulator and Parylene or BCB (Benzocyclobutene) as a stress buffer to reduce the thermal stress between the TSV and Si, thus reducing the fracture driving force. For this purpose, polymeric materials such as Parylene and BCB (Benzocyclobutene) have been used to replace the oxide layer [136, 137]. By using a 2~5 μm thick polymer buffer layer, the thermal stress in the TSV structure can be considerably reduced while its electrical performance can be improved by reducing the capacitive coupling.

For TSVs with a dielectric layer, two interfaces exist, i.e., the interface between the Cu and the dielectric and that between the dielectric and Si. Interfacial crack may grow along either interface. Before evaluating the interfacial reliability, the role of dielectric layer as a stress buffer layer was investigated by comparing the stress distribution along both interfaces. In Fig. 5.4, BCB dielectrics with varying thickness, t_b were considered and compared to fully filled TSV without BCB (t_b=0).



(a)

(b)

Figure 5.4: Stress distribution for varying BCB thicknesses ($D_f = 30\,\mu\text{m}$, and $\Delta T = -250$ ^{o}C): (a) Stress distributuion at the first interface (TSV/BCB); (b) Stress distributuion at the second interface (BCB/Si).

The comparison shows that the radial and shear stress are reduced at both interfaces (Cu/BCB and BCB/Si) with increasing BCB thickness. The results confirm the role of BCB layer as a stress buffer layer. In addition, at relatively deep location from the upper surface, the effect of BCB thickness on radial stress is still distinguishable, while

the thickness effect appears negligible for shear stress. Next, for quantitative comparison of the energy release rate at each interface, steady-state ERRs were determined. To evaluate the energy state for ERR, the stress level which was induced by a thick dielectric layer was first developed. Considering the fact that the explicit form of the stress state for inhomogeneous elastic TSV structure is too complicated to be established analytically, a numerical approach was applied for the calculation. Using appropriate symbols, the stresses in the TSV are:

$$\begin{aligned} \sigma_r &= \sigma_\theta = -q_1 \\ \sigma_z &= q_z^f \end{aligned} . \tag{5.10}$$

The stress field in the dielectric layer is:

$$\begin{aligned} \sigma_r &= \frac{q_1 D_f^2 - q_2 D_o^2}{D_o^2 - D_f^2} + \frac{D_f^2 D_o^2 (q_2 - q_1)}{4r^2 (D_o^2 - D_f^2)} \\ \sigma_\theta &= \frac{q_1 D_f^2 - q_2 D_o^2}{D_o^2 - D_f^2} - \frac{D_f^2 D_o^2 (q_2 - q_1)}{4r^2 (D_o^2 - D_f^2)} \\ \sigma_z &= q_z^d \end{aligned} . \tag{5.11}$$

Note that $-q_1$ and $-q_2$ indicate compressive stresses at each interface (Cu/dielectric and dielectric/Si).

The stress field in the matrix is:

$$\sigma_r = -\sigma_\theta = -q_2 \frac{D_o^2}{4r^2} \quad \text{and} \quad \sigma_z = 0 . \tag{5.12}$$

Where D_f and D_o represent the via diameter and the outer diameter including the dielectric layer; superscripts *f*, *d*, and *m* indicate the fiber, dielectric, and matrix, respectively.

For the calculation of q_1, q_2, q_z^f and q_z^d, the strain continuity at the two interfaces need to be taken into consideration. The out-of plane and circumferential strains should be continuous at each interface (TSV/dielectric and dielectric/Si).

$$\varepsilon_z^f = \varepsilon_z^d \ , \ \varepsilon_\theta^f = \varepsilon_\theta^d \ , \varepsilon_z^d = \varepsilon_z^m \text{ and } \ \varepsilon_\theta^d = \varepsilon_\theta^m . \tag{5.13}$$

Here, the steady-state ERR solution for the interfacial circumferential crack for a TSV structure with dielectric layer is only theoretically provided as follows.

$$\begin{aligned}\Delta U = &\int_0^{\frac{D_f}{2}} U_f^a(r)2\pi r dr + \int_{\frac{D_f}{2}}^{\frac{D_o}{2}} U_d^a(r)2\pi r dr + \int_{\frac{D_o}{2}}^{\infty} U_m^a(r)2\pi r dr \\ &-\left(\int_0^{\frac{D_f}{2}} U_f^b(r)2\pi r dr + \int_{\frac{D_f}{2}}^{\frac{D_o}{2}} U_d^b(r)2\pi r dr + \int_{\frac{D_o}{2}}^{\infty} U_m^b(r)2\pi r dr \right),\end{aligned} \tag{5.14}$$

where, U_f^a, U_d^a, and U_m^a indicate energy state far ahead of the stationary crack tip for the fiber, dielectric, and matrix, respectively. U_f^b, U_d^b, and U_m^b represent the energy states behind stationary crack tip for the fiber, dielectric, and matrix. $U_f^b = 0$ at the first interface, which is the interface between the via and dielectric, while $U_m^b = 0$ at the second interface, which is between the dielectric and Si.

Thus, the steady-state energy release rate for failure at the first interface becomes

$$G_{ss}^I(\alpha, v, \eta^2, \varepsilon_T^2) = \frac{\Delta U}{\pi D_f} . \tag{5.15}$$

And, the steady-state energy release rate for failure at the second interface becomes

$$G_{ss}^{II}(\alpha, v, \eta^2, \varepsilon_T^2) = \frac{\Delta U}{\pi D_o} . \tag{5.16}$$

The superscripts I and II indicate the energy release rate for the first and second interface, respectively.

5.3.2 Effect of dielectric materials

Figure 5.5 plots the energy release rates versus the dielectric layer thickness, in comparison to that of the Cu/Si interface without the buffer layer. The energy release rates for TSVs with practical thicknesses (less than 5 μm) of the dielectric layer are consistently lower than that of the Cu/Si interface. For a very thin dielectric layer, the energy release rate converges to the condition for the fully-filled TSV. Several interfacial fracture energies were measured in the previous papers by other groups [138], which are 12.2 J/m^2 for the Cu/BCB interface and over 24 J/m^2 for the Si/BCB interface. A comparison between the energy release rates in Fig. 5.5 and the respective fracture energy values suggests that delamination is more likely to occur along the Cu/BCB interface.

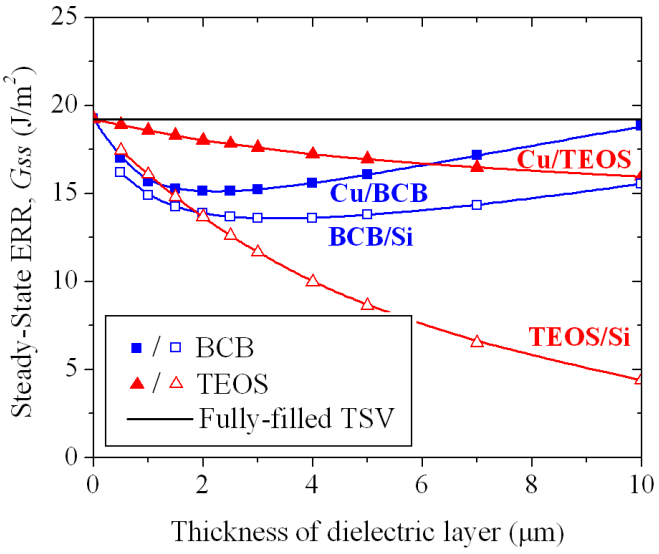


Figure 5.5: Effect of dielectric layer thickness and material property on G_{ss}, where the filled symbol represents G_{ss} at the first interface and the open symbol is for G_{ss} at the second interface ($D_f = 30\,\mu\text{m}$ and $\Delta T = -250\,^{\circ}\text{C}$).

Further optimization on the material and the via structure is thus required to reduce the energy release rate. Either reducing the via diameter or introducing an adhesive layer at the via/BCB interface may be helpful. In addition, the steady-state solution in Fig. 5.5 suggests that an optimal thickness exists for a minimum ERR. The optimal thickness for BCB material that leads to the lowest ERR is around $t_b = 2\,\mu\text{m}$. Meanwhile, the optimal thickness for TEOS is expected to be larger than 10 μm. Even if an optimized thickness hasn't been reached, a layer of TEOS is effective in lowing the ERR sufficiently.

5.4 TSV WITH A NAIL HEAD

5.4.1 Energy release rate

In practice, a hard mask for etching Cu TSVs in silicon substrate often results in a ledge or overhang called 'nail head' or 'overburden' on top of the TSVs (Fig. 2.1d). The nail head could also be allocated to facilitate electrical connection to the upper die on purpose. The presence of the nail head changes the boundary conditions at the triple junction of Cu/Si/Nail head and the outer perimeter of Nail head on top of Si, which in turn changes the stress distribution around both the TSV and Si as shown in Fig. 5.6 and 5.7. In particular, under negative thermal loading ($\Delta T = -250\,^{o}\text{C}$), the concentration of the shear stress along the TSV/Si and the nail head/Si interfaces is increased due to the constraint exerted by the nail head. In addition, the opening stress at the perimeter of the nail head/Si interface possesses singularity. As a result, the concentration of stresses contributes to interfacial failures.

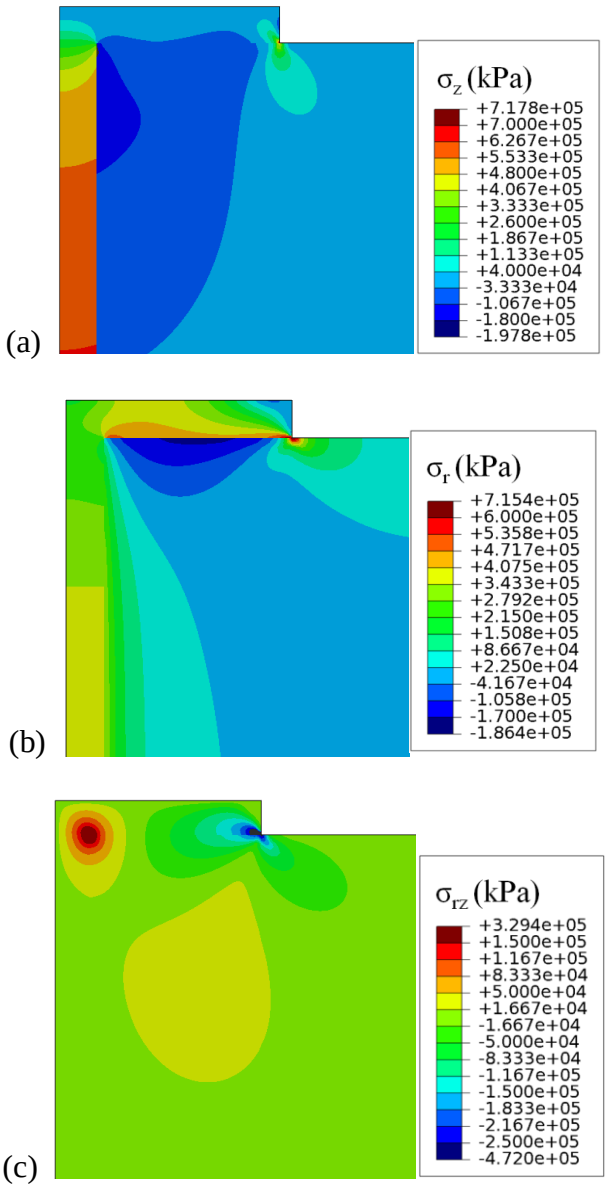
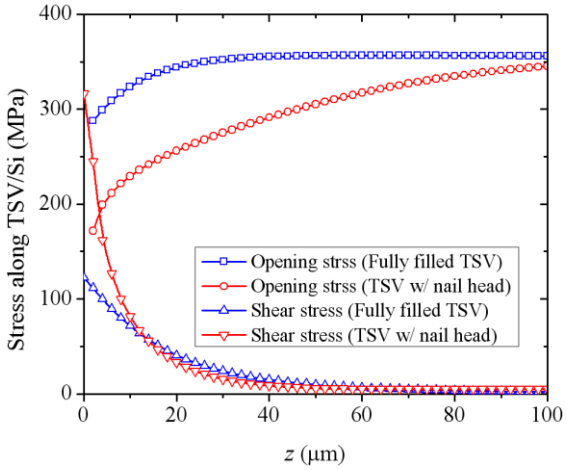
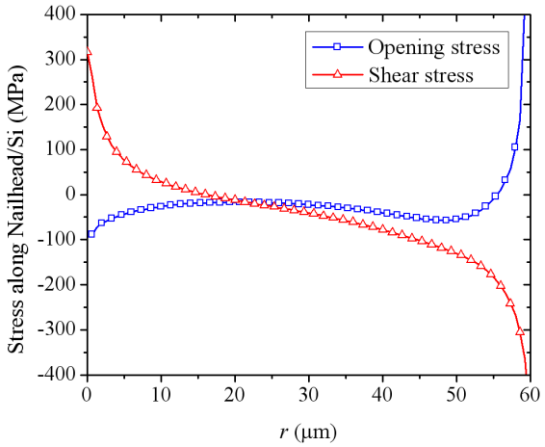


Figure 5.6: Stresses distributions for a TSV with nail-head ($D_f = 30\,\mu\text{m}$, $H_n = 0.5D_f$, $D_n = 6D_f$, and $\Delta T = -250\,^{o}\text{C}$): (a) Out-of plane stress; (b) Radial stress; (c) Shear stress.



(a)



(b)

Figure 5.7: Stresses distributions for a TSV with nail-head ($D_f = 30\,\mu\text{m}$, $H_n = 0.5D_f$, $D_n = 6D_f$, and $\Delta T = -250\,^{\circ}\text{C}$): (a) Stress distributions along the vertical interfacial (TSV/Si); (b) Stress distributions along the horizontal interfacial (Nailhead/Si).

Before discussing further about interfacial failure, the steady-state energy release rate for the TSV structure with nail head under a cooling condition was developed. For the analytic approach, the thickness and diameter for the nail head were assumed to be sufficiently large. The assumption was justified by the comparison with the FEA result. The radial and circumferential stresses far behind the crack tip are zero, while the non-

zero out-of plane stress exists due to the constraint by the nail head. Thus, the stress and strain distributions far behind the crack tip are shown as the followings.

$$\sigma_r = \sigma_\theta = 0$$
$$\sigma_z = E_f \varepsilon_T \quad , \tag{5.17}$$

$$\varepsilon_r^e = \varepsilon_\theta^e = -\nu_f \varepsilon_T$$
$$\varepsilon_z^e = \varepsilon_T \quad . \tag{5.18}$$

Through a similar procedure as used in the previous section, the steady-state ERR solution for interfacial circumferential crack for the TSV structure with the nail head is obtained.

$$G_{ss} = \frac{E_m \varepsilon_T^2 D_f}{4} \left(\frac{(1+\nu_f)^3 (1-2\nu_f)(1-\alpha^2) + (1+\nu_m)(1+\nu_f)^2 (1+\alpha)^2}{\left\langle (1+\nu_f)(1-2\nu_f)(1-\alpha) + (1+\nu_m)(1+\alpha) \right\rangle^2} \right). \tag{5.19}$$

For the effect of nail head on energy release rate, ERRs were compared between fully filled TSV without nail head ($D_f = 30\,\mu\text{m}$) and that with a nail head ($H_n = 0.5 D_f$) under cooling ($\Delta T = -250$ ℃) in Fig. 5.8. As the cooling condition only contributes to the failure of the vertical surface, so that only the vertical crack length (c_1) with zero horizontal crack ($c_2 = 0$) was varied in the calculation.

As the crack propagates along the vertical interface, the ERR approaches to the steady-state solution (Eq. 5.19). The steady-state ERR for TSV with a nail head drops around 30% due to the constraint effect of the nail head. In conclusion, the nail head can be helpful to improve the TSV reliability.

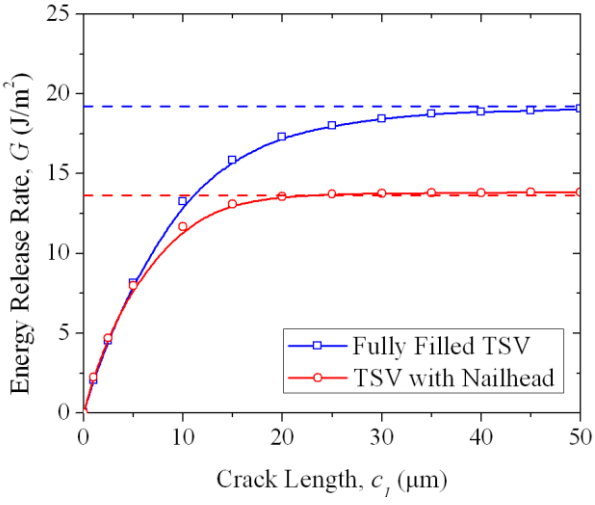


Figure 5.8: Comparison of ERRs between a fully filled TSV and a TSV with nail head ($D_f = 30\,\mu\text{m}$, $H_n = 0.5D_f$, $c_2 = 0$, and $\Delta T = -250$ ℃).

5.4.2 Scenarios for TSV-pop

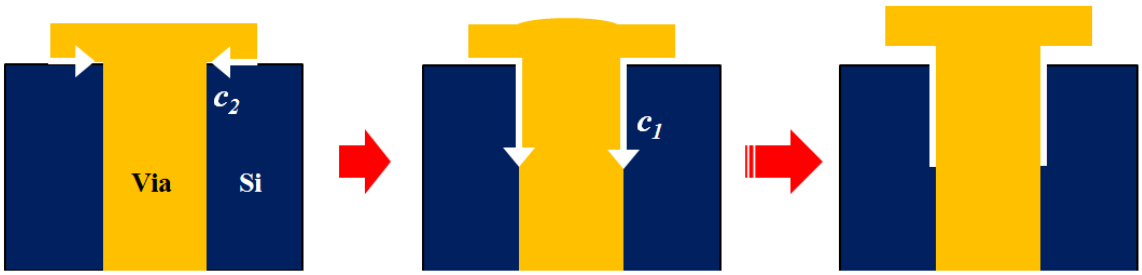
TSV pop-up is a phenomenon of TSV lifting off of the surrounding matrix as schematically depicted in Fig. 5.9. The interface between the nail head and Si is subjected to shearing near the perimeter of the nail head, which may cause delamination at that location. The analysis of the TSVs with nail head has to consider both interfaces, i.e. vertical and horizontal interfaces. If both interfaces fail during thermal cycling, TSV can be extruded from the Si substrate. Here, two scenarios are considered for progression leading to TSV pop-up. For the quantitative study of each scenario, the following parameters are applied; via diameter, $D_f = 30\,\mu\text{m}$, nail height, $H_n = 0.5D_f$ and nail diameter, $D_n = 6D_f$.

Through the comparison of ERR between cooling and heating, it has been observed that the cooling condition produces more serious failure concern than heating. Thus, the first scenario is that during the cooling process ($\Delta T = -250\,^{o}\text{C}$), a vertical crack

(c_1) at the interface (TSV /Si) is generated and reaches a stationary crack size. Then, during the ensuing heating cycle, a horizontal crack (c_2) at the interface between Si and the nail head is generated growing from the junction of the two interfaces toward the outer edge of the nail head (Fig. 5.9a). Technically, a horizontal crack could also start from the outer edge and grow inward; however, the energy release rate in the case was relatively small. Thus, the latter was not considered in the pop-up scenario.

(i) Cooling (ii) Heating (iii) TSV pop-up (Heating)

(a)



(i) Cooling (ii) Cooling (iii) TSV pop-up (Heating)

(b)

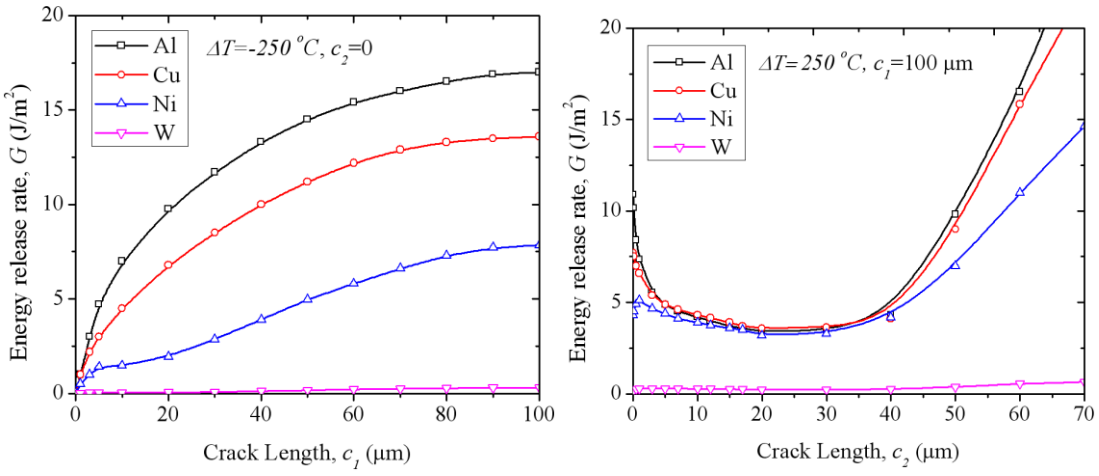
Figure 5.9: Two scenarios for TSV pop-up: (a) Vertical-first scenario; (b) Horizontal-first scenario.

The energy release rates were calculated for the vertical crack during cooling and for the horizontal crack during heating, as shown in Fig. 5.10a. For all TSV materials, the ERR increases with the crack length for the vertical crack and reaches a steady-state

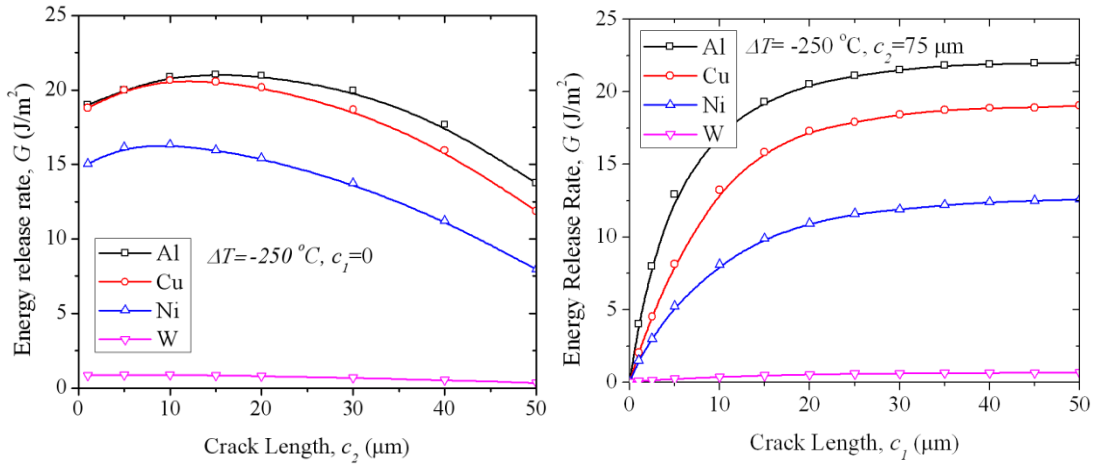
value. With a stationary vertical crack ($c_1 = 100\,\mu\text{m}$), the interfacial energy release rate for the horizontal crack under a positive thermal load ($\Delta T = 250\,^{o}\text{C}$) first decreases and then increases as the crack length increases. The energy release rate starts with a relatively high value for a very short crack. As the crack front approaches the outer edge of the nail head, the energy release rate increases due to the edge effect [76].

For the second scenario (Fig. 5.9b), delamination first occurs at the horizontal interface during cooling, due to the high opening and shearing stresses. Fig. 5.10b plots the energy release rate for $\Delta T = -250\,^{o}\text{C}$. As the horizontal delamination crack eventually reaches the inner junction, delamination continues along the vertical interface. As shown in Fig. 5.10b, the energy release rates for the vertical crack increases with the crack length and is slightly higher than the vertical crack in the first scenario due to the debonded horizontal interface. Subsequently, via extrusion occurs during heating as the interfacial delamination has occurred at both vertical and horizontal interfaces during cooling.

In general, the materials (Al, Cu) with a large CTE mismatch have higher driving force for interfacial delamination. On the other hand, the materials (Ni, W) with low CTE mismatch result in a lower driving force for delamination. When it comes to the possibility for interfacial delamination between the two scenarios, the second one, which has larger initial energy release rate, seems to be more plausible.



(a)



(b)

Figure 5.10: ERRs for TSV pop-up ($D_f = 30$, $D_n = 6D_f$, and $H_n = 0.5D_f$): (a) ERRs for the first scenario; (b) ERRs for the second scenario.

5.5 SUMMARY

In this chapter, the effects of TSV designs and via material properties on the interfacial reliability were investigated. Several TSV structures were considered. Analytical solutions were developed for steady-state energy release rate as the upper-bound estimation for the interfacial fracture driving force. Finite-element analyses were performed to further study the effects of materials and structures on the interfacial reliability of TSVs. For the TSV structure with a nail head, two possible scenarios were discussed for pop-up failure of the TSV. Together, the potential of materials and structure optimization for improving TSV reliability was envisaged as the key for the development of 3-D interconnects.

Chapter 6

Conclusions and Outlook

Three-dimensional (3-D) integration has emerged as an effective solution to overcome the wiring limit imposed on device density and performance with continued scaling. Through-silicon via (TSV), which provides interconnection between the stacked chips, is essential for the 3-D integration. Due to the large mismatch of the thermal expansion coefficients (CTEs) between Cu and Si, thermal stresses induced during processing bring about serious reliability problems. In this context, thermo-mechanical issues of the TSV structures are studied using analytic, numerical and experimental approaches. The analytical research focuses on the interfacial reliability by developing semi-analytic solutions and steady-state energy release rates. Furthermore, a cohesive zone modeling is applied to explain the via pop-up phenomenon due to interfacial delamination. For the stress measurement and material characterization, two measurement techniques, Bending beam curvature technique and Raman spectroscopy, are introduced. For an optimized TSV design, various TSV structures and materials are evaluated.

The 3-D analytical solution characterizes the thermal stresses near the surface where most transistors are fabricated. Away from the surface, the 3-D analytic solution approaches the 2-D plane solution; however, near the surface, the stresses are 3-D in nature. The semi-analytic solution emphasizes the differences in the stress behavior near the surface between the 3-D and the 2-D solutions. The semi-analytic solution serves as a proper approach to understand stress distributions in TSV structures near the surface.

The bending beam technique characterizes the material behavior and evaluates the stresses induced in TSV structures during thermal cycling. This curvature behavior for the fully-filled TSVs is unique in that the curvature-temperature experiences stress relaxation during heating and becomes nearly linear upon cooling. In contrast to the thin film structures, hysteresis loop is absent during thermal cycling for the fully-filled TSV. After the bending beam tests, microstructures of the Cu are studied using focused ion beam (FIB) and electron backscattering diffraction (EBSD). Significant grain growth in the Cu vias was observed, which is correlated to the stress relaxation. After the thermal cycling, via extrusion in the TSV sample occurred, and the phenomenon is explained by local plastic deformation in the Cu vias based on finite element analysis (FEA).

Raman spectroscopy measures a certain combination of the near-surface stresses in the Si. The results obtained from the micro-Raman measurement are compared with the semi-analytic solution and finite element analysis. In particular, the depth dependence of the stress distribution and the effect of elastic anisotropy of Si are investigated by properly interpreting the Raman data. A reasonable agreement between the Raman measurement and the finite element calculation is obtained, demonstrating that Raman spectroscopy is a viable approach to characterize the local stress in the integrated TSV structures**.**

To study the interfacial reliability in TSVs, an analytic approach combining a cohesive zone model and a shear-lag model is developed and compared with FEA simulations. Three distinct stages are discussed for the interfacial behavior. Two critical temperatures are predicted for damage initiation and crack nucleation, respectively. The effects of the material parameters and the via dimensions on the critical temperatures and the associated via extrusion are elucidated.

Analytic solutions for steady-state energy release rates (ERRs) are developed for various TSV structures. Based on these results, the effects of TSV designs and via material properties on the interfacial reliability were elucidated. Together, the potential of materials and structure optimization for improving TSV reliability was envisaged as the key for the development of 3D interconnects.

As an outlook for future works, a few possible studies are suggested. First, in the bending beam tests, the heating rate of 2^{o}C/min was applied, which could provide enough time for material plasticity to occur during thermal cycling. However, if we can suppress the kinetic processes by increasing the heating rate, interfacial delamination, rather than plasticity, could dominate. Therefore, controlling the heating rate could bring about interesting results. Next, additional experiments can be performed to evaluate the stresses in TSV structures and to establish correlations to the results in this dissertation. For example, nanoindentation test could be an interesting method to measure the residual stress in the via after yielding has occurred. Furthermore, AFM can be applied to measure the extent of via extrusion for different thermal loads. These experiments can be correlated with the curvatures from the bending beam tests for stress evaluation. When combined with the microstructure analyses of the Cu via, these experiments could eventually lead to the construction of the Hall-Petch relation. Finally, for TSV interfacial reliability analysis, it is essential to develop experimental methods to characterize the interfacial properties for different materials and structural designs.

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